FAILURE ANALYSIS, MODEL DEVELOPMENT & EYE PATTERN ANALYSIS OF A HI-SPEED TEST FIXTURE

Using a TDR and IConnect® the Interconnect Development & SI Software

by Brian Shumaker – b.shumaker@attbi.com

This application brief demonstrates how to trouble shoot a test fixture whose 50-ohm impedance path takes an impedance dip to 37 ohms somewhere between the BGA connector and the internal driver circuitry of the device, causing the device to fail its signal integrity specifications. Using IConnect, we are able to create an accurate impedance profile (Z-line) from the TDR measurement of the impedance path, eliminating multi-path reflection errors in our TDR reflection waveforms, which makes it possible to troubleshoot and perform further analysis of the test fixture.

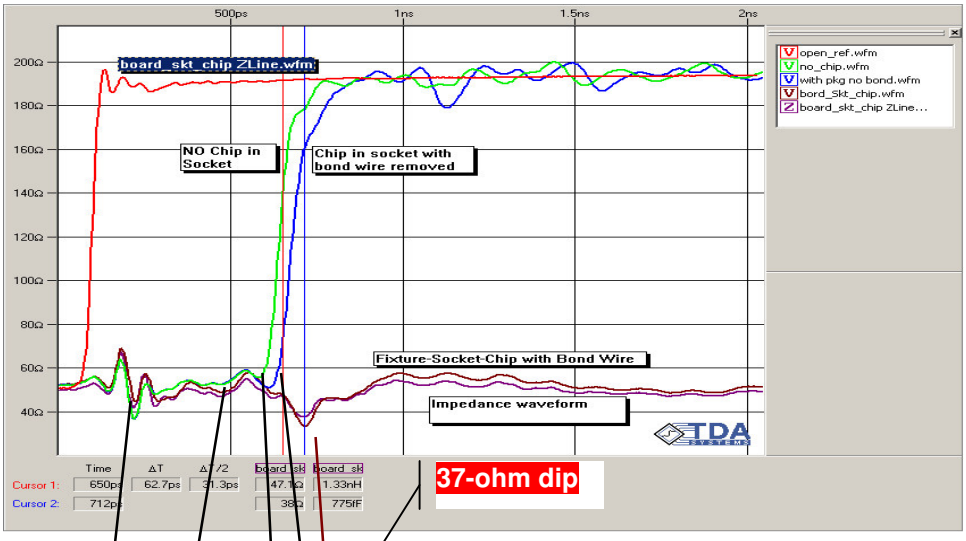
Using IConnect® software on the TDR measurements we wish to:

1. Determine if it the test fixture, the package or the die that the 37 ohm dip occurs.
2. Determine the capacitance of the dip so we can make adjustments in simulation
3. Determine how the driver impedance path affects the eye pattern closure I the test fixture.
4. Develop a verifiable lossy line (RLGC) HSpice model for the fixture, trace and package interconnect path.

Determining location of 37 ohm dip:

The waveform viewer below, generated by IConnect, clearly demonstrates where the impedance dip of 37 ohms occurs and it is located beyond the chip package *within the chip*. We isolated the impedance dip by:

1. Taking a TDR meas. of the fixture connecting the BGA package to the package pad. The package/chip is not attached.
2. Taking TDR measurement with chip package attached to the fixture.
3. Taking a TDR measurement with the die in the package and bond wire removed.
4. Take a TDR measurement with the die bond wire attached to the internal circuitry.



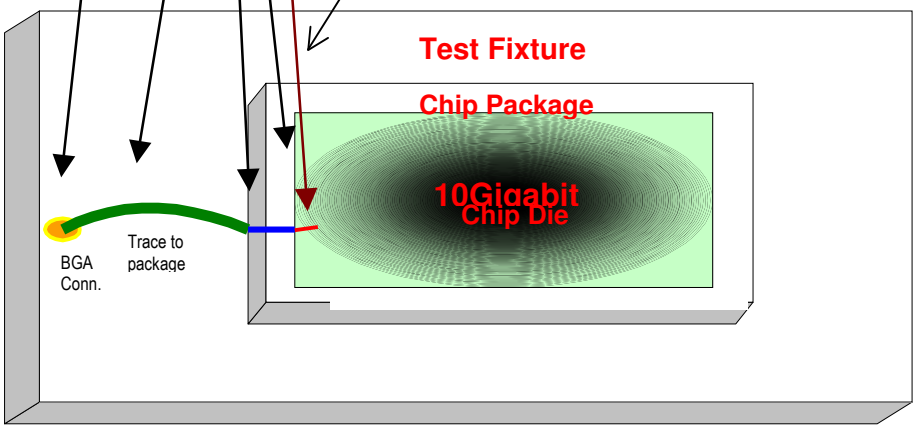


Figure 1
Each TDR measurement was converted to an Impedance waveform (Z-line) with IConnect® to eliminate multi-path reflection errors in the TDR measurements. We now have an accurate impedance waveform to do our failure analysis.

Determining Package & Die Capacitance. To determine the Package Capacitance we use IConnect's *Cself* waveform processing technique. IConnect requires taking a TDR measurement, called the reference waveform, prior to the area you wish to determine its capacitance value. The **no_chip.wfm** in Fig. 2 *package input capacitance.wfm* will be the *reference* at the empty package, and "***with pkg no bond.wfm***" *package input capacitance.wfm* in Figure 2 is the empty package with the bond wire removed. Using the *Cself* function, we compute the Cself to be 420fF as seen in (Fig. 3 **Cself.wfm**). To determine the Die Capacitance, the TDR data for the device with the die inside does not lend itself to using Cself computation because there is a 50-Ohm termination in the die. Using the Z-line approach instead, but first I made sure to understand what portion of the waveform corresponds to what portion of the device as seen in Figure 5 all *capacitance.wfm*.

Looking at this image, you can easily conclude that the capacitance, which we are interested in, is the little dip right after most of the waveforms go up. I can use the single line modeling window in IConnect as seen in Figure 4 Die *capactance.wfm* to get the die capacitance of 856fF by directly reading the values on the impedance (Z-line) profile. This is achieved by bracketing the dip as seen by the yellow areas on each side of the dip then choosing the CL topology and setting the impedance to mean and the value for C will be calculated as seen in Figure 4 Die Capactance.wfm. Based on this TDR data, we extracted the package capacitance of 420fF and die capacitance of 850fF.

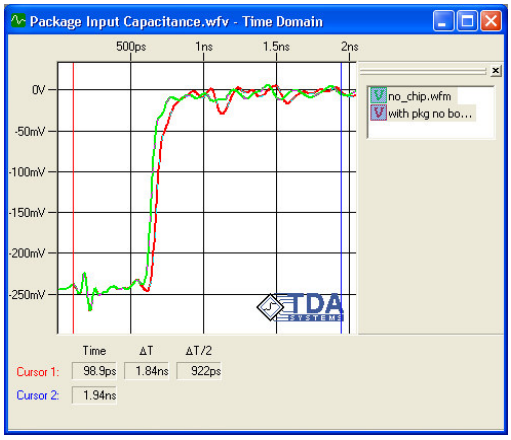


Figure 2

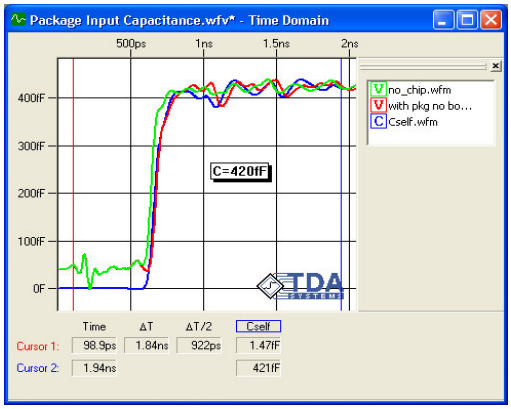


Figure 3

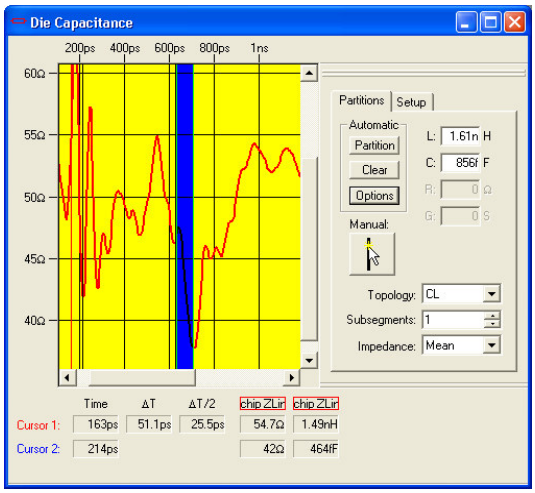


Figure 3

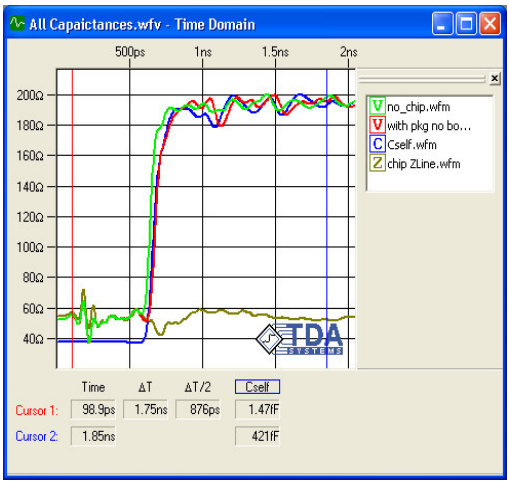
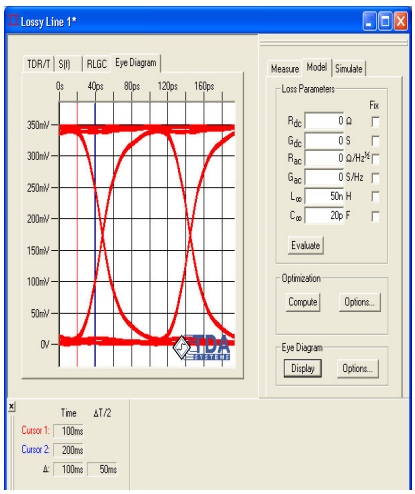
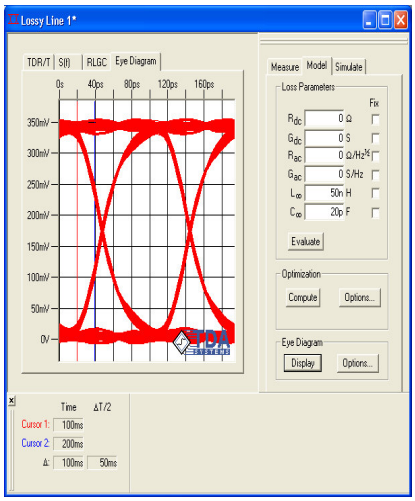


Figure 5

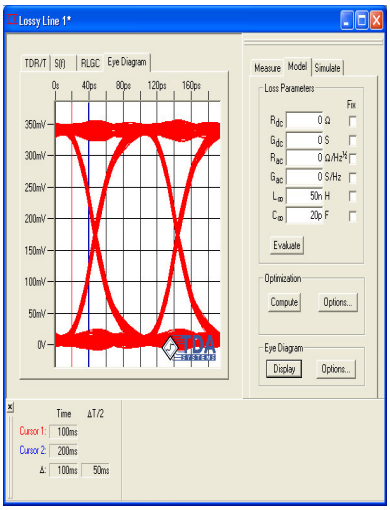
Finally, using the IConnect's lossy line model generator, the TDR waveforms and reference waveforms we can produce a lossy line model and eye pattern for the for each of these impedance paths. With cursors you can measure the eye closer for each interconnect path and determine the effect the interconnect paths will have on your design and if each impedance path will cause your device to fail its signal integrity parametric performance. Refer to IConnect's Help/Getting Started/ Lossy Line Modeling Session for examples on how to create a Lossy line model and eye pattern.



Test Fixture, no Package or Die



Fixture, Board & Package, no Die

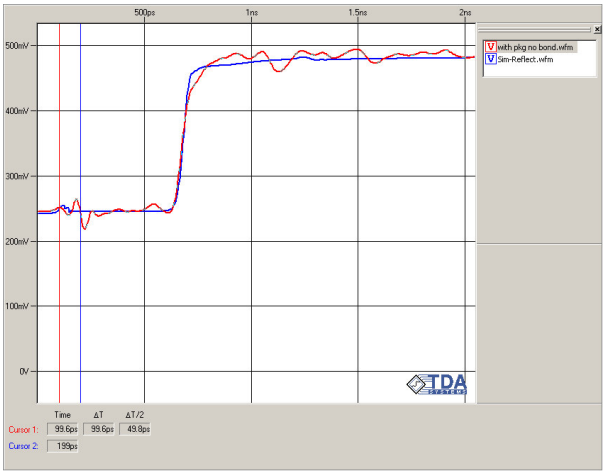


Fixture, Board, Package with Die

```
* Time Domain Analysis Systems:  IConnect
* Version 2.0.3  Evaluation Edition

* File Created: February 27, 2003 at 10:28AM
* Created By: Administrator

* Format: Model
* Type: Lossy Line

* == Begin Header ==

* Termination: Open
* Reference Waveform: ..\board to pkg\open_ref.wfm
* Reflection Waveform: ..\board to pkg\with pkg no bond.wfm
* Parameters: Rdc=48.8m, Rac=40.5u, Linf=14.5n, Gdc=4.98n, Gac=840f,
Cinf=5.07p
* Format: W-Element
* Length: 1
* Syntax: HSpice
* Name: Automatically Generated

* == End Header ==

.subckt Lossy_Line_1 port1 port2 gnd_

W1 N=1  port1 gnd_  port2 gnd_ RLGCMODEL=Lossy_Line_1_Model L=1

* RLGC values for W element
.MODEL Lossy_Line_1_Model W MODELTYPE=RLGC N=1
+ Lo=1.45e-008
+ Co=5.35e-012
+ Ro=0
+ Go=0
+ Rs=4.05e-005
+ Gd=1.12e-012

.ends
```

At left, is the HSpice model listing for the impedance path of the fixture, package and die with the bond wire removed created by IConnect's lossy line model generator.

Below is the **simulated output waveform** for the lossy line model overlaying the impedance path with **no package and bond wire removed** for easy comparison and validation of the simulated waveform. Only lossy properties (R, L, G, C) are reflected in the simulated waveform. If time depended information is required, with IConnect, you can create a distributed composite model that combines both lossy and loss-less models together.



SUMMARY

By using IConnect and a TDR oscilloscope we successfully isolated the 37-ohm low impedance dip to be located inside the die and not the fixture or package. We isolated the problem by taking TDR measurements, converting each measurement to an impedance waveform (Z-line) of:

1) Only the test fixture,
2) The fixture with the package installed,
3) The package and die installed without the bond wire attached, and finally,
4) With the die installed with the bond wire attached. The waveforms are stacked atop another in Figure 1. and it clearly shows that the 37-ohm dip is located just inside the die. This excessive capacitance may be related do to the insulation material applied to the bond wire which is adding excessive capacitance to the input to the driver causing the device to fail its signal integrity parametric specifications.

Since an impedance dip indicates higher capacitance (Z=Square root (L/C)), with IConnect, we were able to determine the exact package & die capacitance. The 850fF is too high and with this information we can make adjustments to our simulation and it also provides the information that linked the problem with the isolation around the bond wire.

With the TDR measurements already obtained from our fixture, package and die IConnect allows us to generate eye patters for the driver path to validate that our fixture, package or die will not degrade the DUT performance when we later perform at-speed functional tests. Also, from these measurements we were able to generate and validate HSpice models for the fixture, assuring the impedance of the signal path will maintain precision 50-ohm impedance required for our DUT. Having accurate models for our fixtures and interconnect systems we will not have to do additional board turns saving valuable engineering time and development expenses.

FOR MORE INFORMATION ON ICONNECT VISIT:
TDA SYSTEMS
http://www.tdasystems.com