Application Note

Signal Trace and Power Plane Shorts Fault Isolation Using TDR

Techniques for locating open faults with Time Domain Reflectometry (TDR) oscilloscopes have been successfully demonstrated in papers presented at ISTFA 1999 [1] and 2000 [2]. It has been shown that obtaining the true impedance profile using TDA Systems' IConnect TDR software [2], or other implementations of the impedance deconvolution algorithm, allows locating the faults in the packages more repeatably and predictably, and in [2] a number of techniques using the impedance profile have been presented. For example, one of the key impedance profile features differentiating an open fault in the package or bondwire from an open fault in the die itself is a dip in the impedance profile corresponding to an input die capacitance and presenting itself shortly before the open impedance signature. The presence of this characteristic dip in the impedance profile indicates a good connection to the die, whereas its absence indicates a problem in the package structure. Such a capacitive signature can be observed much more readily on the impedance profile waveform than on a raw TDR waveform.

In this report our focus is on locating short failures, using TDR-based fault isolation system. The failures include signal-to-ground shorts and plane-to-plane shorts. Examples of plane-to-plane shorts may be a power plane to a ground plane short, or a short from one power plane to another, inside the package or inside the die.

Signal-to-Ground Short Failures

Experiments demonstrated that a signal to ground plane short can be located relatively easily using the same techniques as those used for locating an open fault. Since the trace has certain amount of characteristic impedance, a short failure will clearly exhibit itself on the true impedance profile, as a rapid decrease in impedance until this impedance reaches zero Ohm.

Since in Figure 1 we can observe that the short waveform goes towards zero Ohm right where the bare package substrate waveforms goes into an open (high impedance), and right before the good device waveform goes to the die capacitance, we conclude that the short is located at or near the connection to the die.

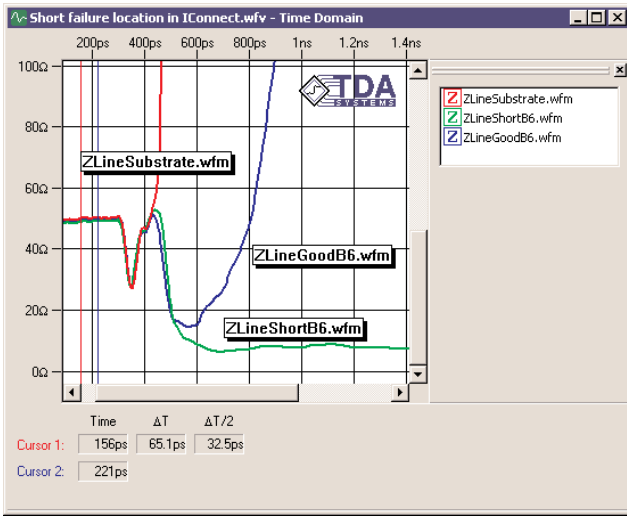

Figure 1. Locating a signal to plane short failure using the impedance profile signature. By comparing the short waveform (ZlineShortB6.wfm) to the substrate waveform (ZlineSubstrate.wfm), one easily concludes that the short is located near the connection to the die

One can extend the technique reported in [2] to determine the average dielectric constant E_r through the package using the following equation:

$$V_{prop\ average} = \frac{V_c}{\sqrt{\varepsilon_{r\ average}}} \qquad (1)$$

where V_{prop} average is the average signal propagation velocity through the package, V_c is the speed of light in vacuum. We can rewrite this equation as

$$\varepsilon_{r\ average} = \left(\frac{V_c}{V_{prop\ average}} \right)^2 \qquad (2)$$

In our example, the electrical length is 63ps, and the physical length is 8.7mm, which gives average propagation velocity of 7.24ps/mm or 0.138mm/ps. Using this number, and knowing that the speed of light in vacuum is 0.305 mm/ps, we obtain the average E_r of 4.9. Then, one can display the data in IConnect TDR software as impedance versus physical time.

The actual dielectric constant (E_r) for the substrate has been measured to be 4.2 at 1 MHz, which comes from the material property data provided by the substrate vendor. Using E_r=4.2 to recalculate

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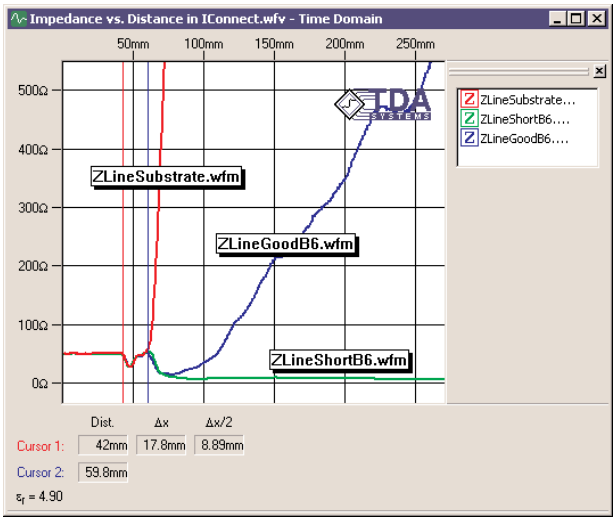

Figure 2. Impedance vs. distance in IConnect TDR software. The fault occurred about 63ps or 14mm inside the package

the physical length, the measured total length of the trace is 9.4 mm, which is very close the actual CAD layout length of 8.7 mm (~8% error). It is a very good correlation, considering that the E_r would be higher at higher frequency for the TDR measurement, and that we are looking for the average E_r through the whole package. The localized E_r variations, non-homogeneity, effects of different conductor shape, all contribute to the difference between the vendor supplied E_r and the measured value. However, the overall correlation we observe is considered to be quite good.

Plane-to-Plane Short

Locating a plane-to-plane short, such as ground plane to power plane short, is a more difficult task. In case of a signal trace, the characteristic impedance of such trace is normally in the range of 30 to 80 Ohms, and observing the change from this range to zero Ohm in the impedance profile waveform is relatively easy. The power plane, however, presents much lower impedance to the TDR signal, typically on the order of less than 0.5-2 Ohm, and the change from that impedance to zero does not always allow the failure analyst to use the impedance profile effectively to find the exact location of the short between the planes using either time or distance.

In this paper, however, we propose two comparative techniques for plane-to-plane short location, both based on secondary information in the TDR data. One technique looks for the difference in the secondary reflections in the TDR waveform, and can be performed with the raw TDR data or using the true impedance profile. The second technique looks at the inductance of the current return path, which can be computed in IConnect TDR software, based on the JEDEC standard described in [3] and [4]. Smaller inductance indicates a shorter distance to the short, and by comparing the failing device measurement to that of the good device and a shorted package substrate, one can determine the relative position of the short failure. For both techniques, repeating the measurements multiple times to ensure good repeatability is key to finding a fault.

Test Example

Consider the following simple test board example (Figure 3).

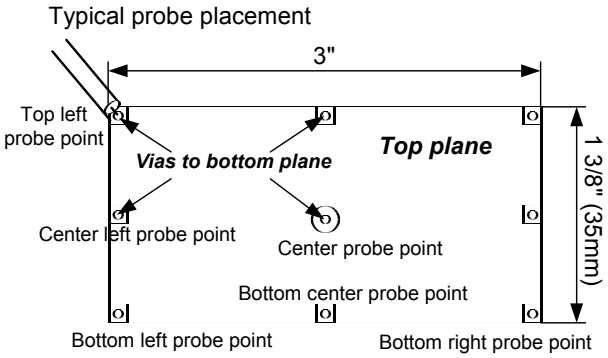

Figure 3. Test board for plane-to-plane short failure location. The board consists of two planes that can be probed with TDR at multiple locations at one side of the board and shorted at another side

This test board consists of two planes, which have via probe point at multiple locations on the board. Using these vias, the failure analyst can perform TDR measurements of the two planes on one side of the board, while at the same time shorting the planes at the other side and attempting to locate the position of the short. The board is about twice the size of a typical BGA package, which makes it an easier test case. The Table 1 summarizes the expected closeness of the shorted probe point to the top left probe point, where the TDR signal is applied, based on visual analysis of the board.

Table 1. Physical closeness of short point to the top left probe point (closest, 1 to farthest, 8), based on visual analysis

	Left	*Center*	*Right*
Top	X	2	6
Center	1	4	7
Bottom	3	5	8

We applied signal every time at the same location (top left probe point), while creating a short between

the planes by connecting the via from the bottom plane to the top plane contact. We shorted the two planes together at each of the remaining probe point locations and acquired the corresponding TDR waveform (Figure 4).

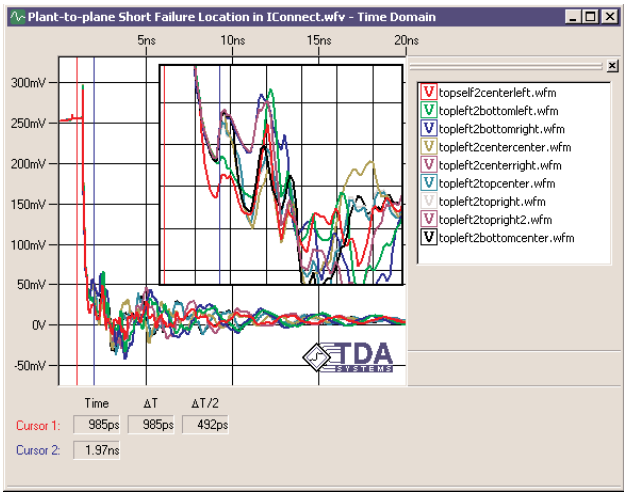

Figure 4. Locating plane-to-plane short on the test board. The fault location is based on the secondary TDR measurements, such as secondary reflection delay and inductance measurement

As one can see from Figure 4, there is little delay between the different waveforms. The inset, however, demonstrates, that the waveforms do exhibit difference in position and waveshape. If a failure analyst tried to analyze this difference and determine which short is closer to the point where the TDR signal is applied, the following order could be established as shown in Table 2 (from closest short to the probe point to the farthest).

Table 2. Electrical closeness of short point to the top left probe point (closest, 1 to farthest, 8), based on TDR measurement

	Left	*Center*	*Right*
Top	X	4	5
Center	1	3	7
Bottom	2	6	8

By comparing these results with the expected results from Table 1, a failure analyst can observe a good correlation. The only questionable result is that the center top probe point comes after the center point. The difference between the two waveforms corresponding to those probe points, however, is small, and can be attributed to measurement repeatability issues.

To confirm our conclusions, we compute the total inductance of the plane for each measurement in IConnect TDR software. This measurement is a good figure of merit for the current return path through the plane, which, in turn, is a good indicator of where the short may have occurred.

The following table summarizes the inductance data, listing the shorted probe point inductance measurements from the smallest to the largest. All the inductance measurements have been in 2-4 nH range.

Table 3. Electrical closeness of short probe point to the top left probe point (from smallest inductance, 1 to largest, 8), based on inductance measurements in IConnect TDR software

	Left	*Center*	*Right*
Top	X	3	4
Center	1	5	7
Bottom	6	2	8

Again, the center point and the bottom left point are outliers, but otherwise this table correlates well to the Table 1 of expected physical closeness.

These "outliers," or incorrect data points, may come from some minor details and changes in the current return path between the planes. Vias and other plane openings, such as those on the test board in question can affect this return path. All these issues indicate that the failure analyst must apply these techniques to plane-to-plane short analysis with the good understanding of the TDR measurement technique, and must study the layout and structure of the package carefully. Repeated measurements may be necessary in order to prove the actual location of the short.

Measurements of the Package Under Test

The technique described in section Test Example on page 2 has been applied to the measurement of a sample package. The package has two planes, which have been connected via the Electro-Static Discharge (ESD) diodes on the periphery of the die. These ESD diodes result in some additional resistive connection between the planes when the TDR signal is applied to the planes and reaches the diodes. Three samples of the same package type have been tested: a good one, a failing one (plane-to-plane short failure) and a bare substrate, with the two planes shorted at the end of the substrate for reference. The corresponding waveforms are shown on Figure 5.

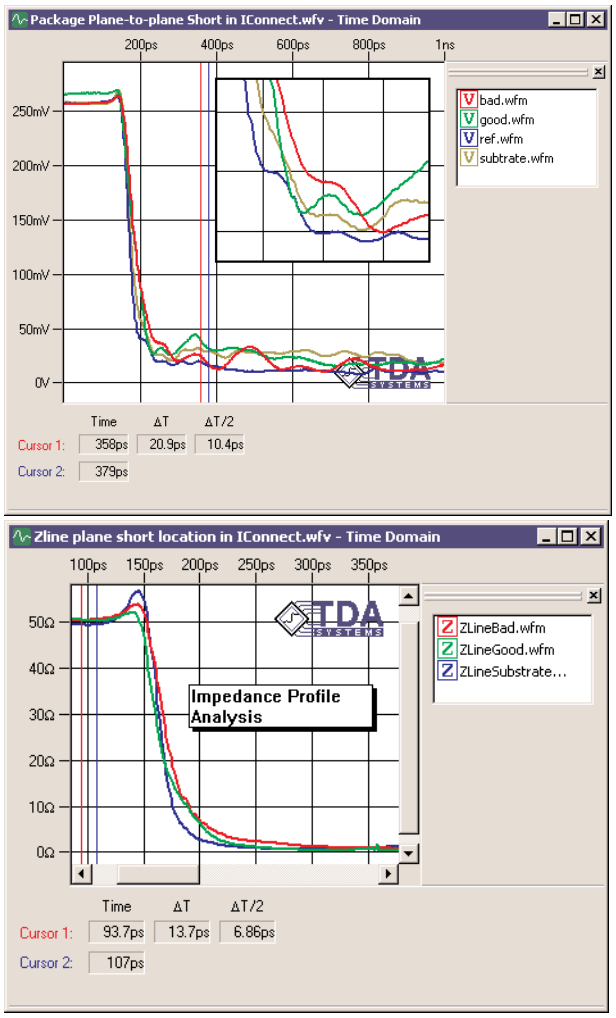

Figure 5. Locating a plane-to-plane short in the BGA package using raw TDR data (above) and the true impedance profile (below). The failure position appears to be on the die

From Figure 5, the relative position of the 4 waveforms is as follows:

1 - ref.wfm
2 - substrate.wfm
3 - good.wfm (good die)
4 - bad.wfm (failing device)

This order leads us to the conclusion that the short between the planes occurs on the die. This is further supported by the inductance analysis:

Substrate.wfm - 400 pH
Good.wfm (good die) - 600 pH
Bad.wfm (failing device) - 800pH

In Figure 5, it appears that the known good device is also shorted to ground. In fact, a relatively large capacitance between the planes will appear to present a short signature for the first few nanoseconds, but then the discharge of this large capacitor will eventually (after a few tens of nanoseconds) return the TDR waveform to the voltage level corresponding to an open signature.

The next step after the failure has been located with the TDR is to use other, possibly destructive, analysis techniques, in order to determine the cause of the failure. In our case, lapping of the die to locate the short inevitably led to the disappearance of the short, which indicates that our TDR-based analyses are correct, even though we have not been able to establish the physical cause of the short.

Summary and Conclusions

In this paper, we have analyzed the application of the TDR measurement techniques and the true impedance profile to finding the location of signal-to-ground and plane-to-plane shorts in electronic packages. Locating a signal-to-ground short has been shown to present little difficulty over a comparable open fault locating task. Plane-to-plane shorts, however, present additional challenges, which require more attention to the repeatability and accuracy of the measurements. However, with the true impedance profile and plane inductance analyses, the claim of impossibility of locating a plane-to-plane short is effectively challenged in this paper.

Further study to determine the failure location more accurately can be done by applying the TDR source from different corners of the package planes in order to triangulate the failure.

References

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[3] Guideline for Measurement of Electronic Package Inductance and Capacitance Model Parameters, - JEDEC Publication #123, JC-15 Committee, October 1995
[4] D.A. Smolyansky, "TDR Techniques for Characterization and Modeling of Electronic Packaging," - High Density Interconnect Magazine, March 2001, Part 1 of 2

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