Application Note

TDR Characterization of ATE Fixture Boards and Sockets

Introduction

Signal integrity in ATE fixture boards, also referred to as load boards or Device Under Test (DUT) interface boards, is a key part of achieving a high-quality, low noise test environment. At-speed testing places severe requirements on the quality of load boards, demanding minimal signal distortion at speeds of several hundred megahertz and sub-nanosecond rise times. Distortion of the test signals delivered to the DUT and the signals received by the tester comparators results in test errors, rejection of working parts, and, even worse, acceptance of faulty ones, costing the manufacturer thousands, or even millions or dollars.

In this article, we will discuss characterization of ATE fixturing using TDR measurement methodology, and offer some suggestions on how this characterization data can be used to avoid unnecessary test failures. As a result of careful ATE load board analysis, more accurate production test limits can be set. Test engineers can use detailed load board characterization data to model the device performance accurately in the test environment, and to ensure accurate interpretation of test results. With accurate characterization data, test engineers can improve overall test yield for their ICs, resulting in significant savings for the IC manufacturer.

Load Board Characterization

A load board typically contains a test socket or contactor for connecting the DUT to the test system. The test socket is mounted on a controlled-impedance printed circuit board, which is mounted on an ATE test head and uses high-performance connectors to connect to ATE pin electronics. Because of typically large pincount of test devices, most load boards are quite complex internally, running 10 to 18 layers, including signal, power and ground layers. In order to understand signal distortion as the signal propagates through the load board, all the components of the ATE load board need to be characterized. Connector and test sockets introduce small inductive and capacitive discontinuities that need to be taken into account as well.

TDR measurement traditionally has been used to determine impedance in high-speed digital boards [1], [2], and is a natural choice for characterization of the ATE load boards. However, performing a TDR measurement on all the signal paths in the ATE load board is time-consuming. To save engineering time and achieve the desired characterization results in the most expedient way, one or several critical signal paths on the load board must be chosen. The selection of the critical path can be based on a visual inspection of the board layout, the designer's knowledge about the board components, and experience of the load board designer. If the board is analyzed as a suspect component leading to test failures, a device pin with an unpredictable failure pattern may be the one that requires the most attention, and the load board path to that pin can be designated as the critical path.

The TDR data for the load board by itself is quite useful, because it shows how the board distorts the TDR signal. One has to keep in mind, however, that the rise time of TDR oscilloscopes is quite fast, on the order of 30 to 40ps, and the real-life tester and device rise times are much slower. At a rise time of 250ps, the signal distortions due to inductive and capacitive discontinuities are smaller (Figure 1).

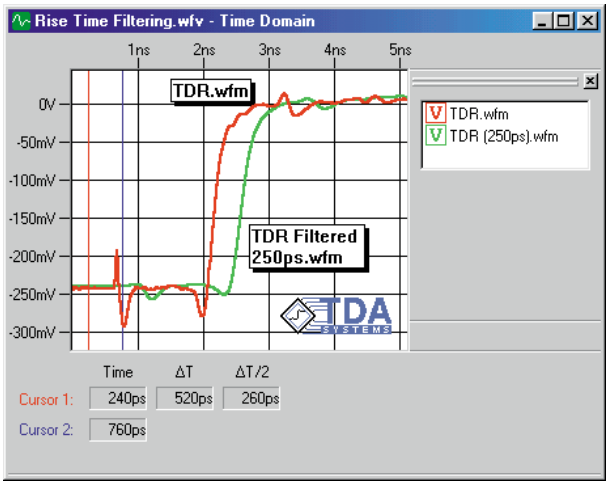

Figure 1. Rise time filtering is important when performing TDR characterization of the load board. At a more realistic slower rise time of 250ps, the discontinuities due to connector are not as large as they are at a 35ps TDR oscilloscope rise time

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If the load board has more than a single impedance trace on a single board layer, the TDR measurement by itself will not provide accurate impedance measurement information because of the multiple reflection effects present in the TDR waveform [3], [4]. The multiple reflections are due to the re-reflection of the signal inside the load board itself between different discontinues. Even in the simple example of a single impedance load board, the multiple reflections are present due to connector and socket discontinuities and may decrease the accuracy of the measurements (Figure 2). The true impedance profile, however, can be computed from the TDR waveform using the impedance deconvolution technique discussed in [3] and [4].

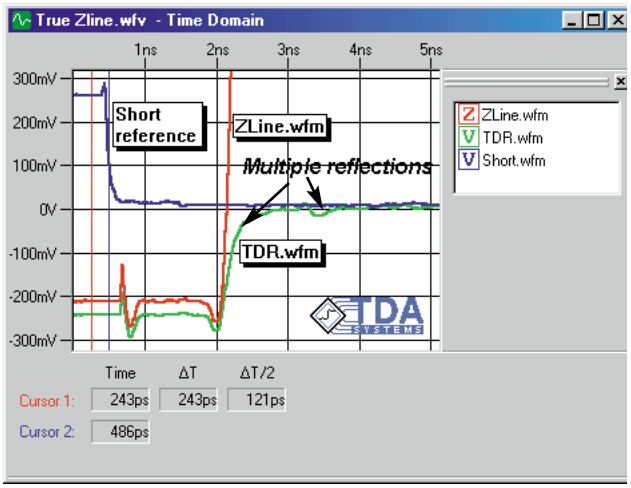

Figure 2. Multiple reflections in the TDR waveform. The true impedance profile (Zline) is computed in IConnect software, and allows the test engineer to extract the equivalent circuit model for the load board interconnect easily

The impedance deconvolution algorithm is implemented in TDA Systems' IConnect TDR software and is applied as follows: the true impedance profile is computed from the TDR waveform and the reference short or open waveform. The reference waveform defines the reference measurement plane for the board trace under test. The impedance profile of the board, computed from the TDR measurement (Zline.wfm), reveals a DUT interface with a well-controlled impedance (Figure 2).

Load Board SPICE Model Extraction

In addition to obtaining accurate impedance information, it is important to provide a complete SPICE or IBIS model of the load board interconnect so that the signal distortion could not only be observed, but also predicted in simulations. The true impedance profile, once computed, provides an easy path to obtain such SPICE models for the load board interconnects.

Based on the true impedance profile, IConnect software can automatically save a SPICE equivalent circuit model for the critical path under consideration (Figure 3). Trace impedance and delay are computed directly, and parasitic inductance and capacitance are computed from the impedance profile using the following equations:

$$C = \frac{1}{2}\cdot\int_{t_1}^{t_2}\frac{1}{Z(t)}dt \qquad L = \frac{1}{2}\cdot\int_{t_1}^{t_2} Z(t)dt \qquad (1)$$

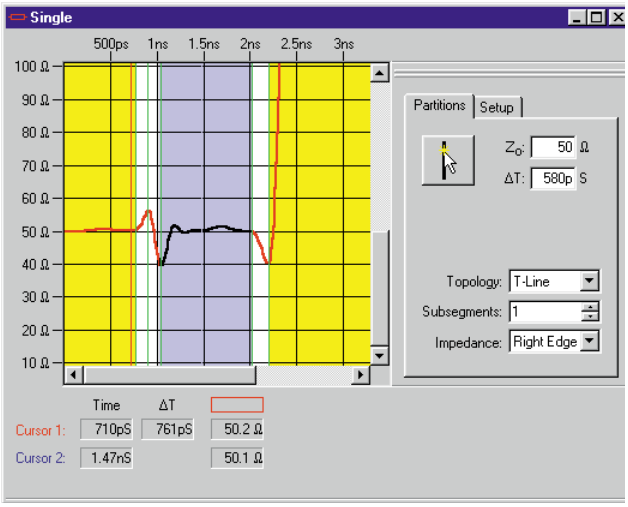

Figure 3. DUT interface board impedance profile. The impedance profile is partitioned into sections, and the equivalent SPICE model for the board is computed by IConnect TDR software

The equivalent SPICE model computed by IConnect is listed below.

Sample SPICE Model Listing Generated by IConnect Software

```
* Z Waveform: ZLine.wfm
* Syntax: PSpice/Hspice/Berkeley SPICE3, compatible with any SPICE
* Name: Automatically Generated
.subckt Single 1 2 3
****** Partition #1
  l1  1  4 1.77n
****** Partition #2
  c1  4  3 1.76p
****** Partition #3
  t1  5  3  6  3 Z0=50.7 TD=580p
****** Partition #4
  c2  6  3 1.99p
  l3  6  2 3.38n
.ends
```

To check the validity of the board model, IConnect TDR software comes in handy again because it allows the test engineer to recreate the TDR incident step for the simulation, using the reference short waveform. Recreating the TDR incident step in simulation is important in order to ensure one-to-one comparison of the measurement for the load board and the simulation, the latter obtained using IConnect-generated model for the load board and the TDR source. That way, if there are discrepancies between simulation and measurement, they can only be caused by the model itself, which can be easily fine-tuned in IConnect. The reference short waveform is the same as that used to compute the true impedance profile before. As a result, the test engineer can simulate the model extracted above using the direct interface from IConnect to SPICE simulators, and the resulting comparison of simulated and measured data is automatically generated by IConnect. Figure 4 below shows excellent correlation between simulation and measurement, which is achieved even at a very fast 35-40 ps rise time.

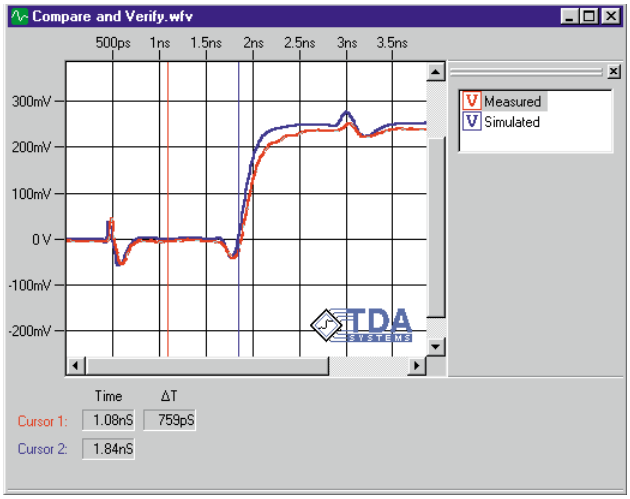

Figure 4. Comparison of simulated and measured data for the DUT interface board. Excellent correlation is achieved even at a very fast 35-40ps TDR rise time

Once the model for the critical path is validated, the fixture designer can provide the test engineer with meaningful and accurate equivalent circuit model data, which can be used to predict the signal distortion in the load board. Additionally, if required by the test engineer, he or she can compute S-parameters for the critical path interconnect or spectrum for the signal in question. For example S_{21}, computed in IConnect based on the TDT (Time Domain Transmission) measurement, can provide information about the insertion loss of the load board under test.

Differential lines in the ATE fixtures can be characterized similarly, using the approach outlined in [5]. Even and odd mode impedance profiles, computed from differential and common mode TDR measurements, can quickly provide a distributed coupled line model, which can accurately predict the signal integrity issues in the ATE fixture.

Connector Characterization

Connectors are key to the overall DUT board performance, since it is significantly harder to maintain controlled impedance through a connector and connector-to-board interface than through the board itself. The fixturing for the TDR measurement of a connector consists of a high-performance coaxial cable soldered directly to a connector pin. The connector is mated to the other connector half. TDR measurement of the connector has been processed in IConnect software to remove multiple reflection effects from the TDR waveform and to compute the true impedance profile for the connector trace. The true impedance profile makes it easy for the test engineer to analyze the connector for specific discontinuities (see Figure 5 below).

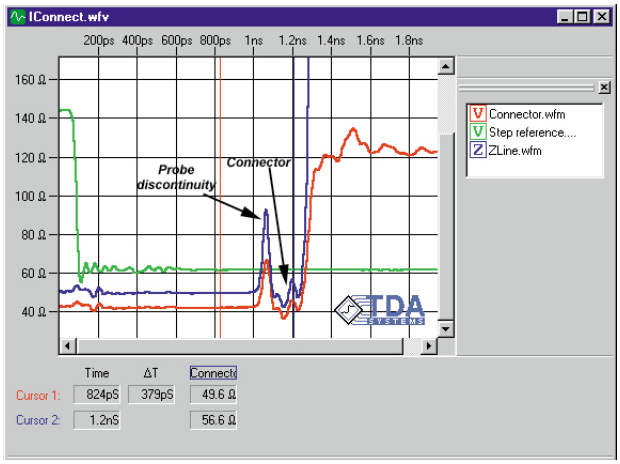

Figure 5. Analyzing the load board connector. True impedance profile makes it easy to distinguish different segments of the connector and the fixturing used in the connector measurements

To analyze the connector performance at the device specific rise time, the rise time filtering was applied again, this time using a 175ps filter (Figure 6).

The impedance profile, filtered at 175ps rise time filter, shows that the probe discontinuity is negligible and the connector exhibits controlled impedance behavior. The equivalent SPICE model computed by IConnect consists of a 100ps long transmission

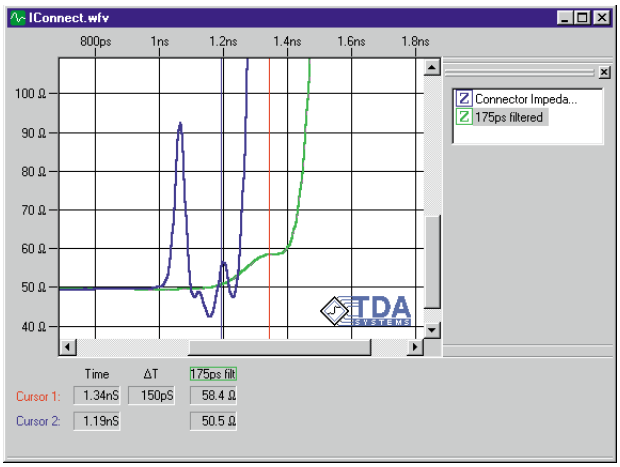

Figure 6. Impedance profile of a connector filtered at 175ps

line of 58 Ohm impedance. This model is valid up to the 175ps filter rise time as defined above. The equivalent 3dB frequency range of validity can be estimated as approximately 2Ghz, using the following equation:

$$f_{3dB} < {0.35}/{t_{rise}} \qquad (2)$$

Based on the reference short measurement, test engineer can recreate the TDR incident step in IConnect. Comparing the simulation results to a measurement verifies the accuracy of the model.

Test Socket Characterization

Test socket characterization is important as part of the overall signal path characterization in the ATE environment, since sometimes the test socket parasitics can be high. Socket vendors frequently provide the parasitic inductance, capacitance and resistance data; however, it is often important to validate this data in the specific test environment.

Typically, a lumped (RLC) model for the test socket parasitics is used, which is valid when the electrical length of the socket is small compared to the rise time of the test signals:

$$t_{socket} < {t_{rise}}/{6} \qquad (3)$$

The electrical length of the socket t_{socket} can be measured by TDR as part of the characterization work. The factor of 6 in this equation is somewhat arbitrary, but widely used by high-speed designers as a rule of thumb.

Single-ended TDR techniques

The test socket can be characterized following the procedure for characterization of electronic packaging outlined in [6], using the measurement setup shown on Figure 7.

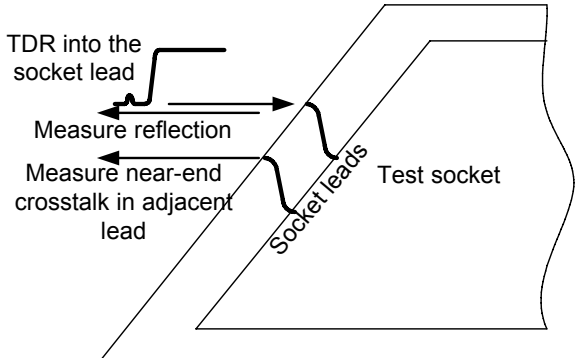

Figure 7. Measurement setup for single-ended TDR characterization of an ATE socket. The socket leads must be shorted to ground on the inside of the socket for inductance measurements, and left open-ended for capacitance measurements

Both self and mutual inductance and capacitance can be computed using this *Guideline* [6]. For example, for capacitance computation, the test engineer will send a TDR step into a socket lead and acquire the DUT waveform (W_{TDR}). By removing the socket from the board and performing a TDR measurement into the same trace, the test engineer obtains the reference open waveform (W_{open}). If the socket is not mounted on the board and is accessible by a ground-signal probe, then the reference measurement will constitute raising the probe and performing a TDR measurement into the open air.

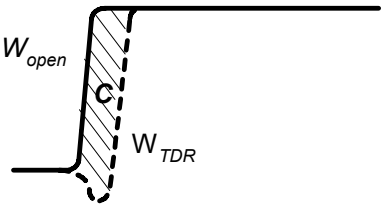

Figure 8. Self-capacitance computation

Then the self-capacitance can be computed as:

$$C_{self} = \frac{1}{2 \cdot Z_0 \cdot V} \cdot \int_0^{\infty} (W_{open} - W_{TDR})\,dt \qquad (4)$$

where V is the TDR voltage incident at the lead under test, normally half the TDR source amplitude, and Z_0 equals the characteristic impedance of the

measurement system, 50 Ω for currently available TDR instruments.

Mutual capacitance of the socket can be computed based on the near-end crosstalk measurements as follows:

$$C_{mutual} = \frac{1}{2 \cdot Z_0 \cdot V} \cdot \int_0^{\infty} (W_{induced} - W_{background}) dt \quad (5)$$

where $W_{background}$ is just a background noise waveform, acquired with no TDR stimulus on either of the lines.

Self and mutual inductance can also be computed using the following equations:

$$L_{self} = \frac{Z_0}{2 \cdot V} \cdot \int_0^{\infty} (W_{TDR} - W_{short}) dt \quad (6)$$

$$L_{mutual} = \frac{Z_0}{2 \cdot V} \cdot \int_0^{\infty} (W_{induced} - W_{background}) dt \quad (7)$$

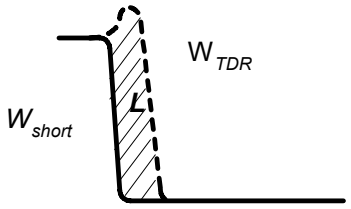

Figure 9. Self-inductance measurement

The computational procedure for self and mutual L and C extraction using equations (4)-(7) is also automated in IConnect TDR software.

Differential techniques: even and odd impedance profiles

The fixture for inductance measurements as defined in [6] is more complex than the fixture for capacitance measurement, and requires making a short connection on the inside of the socket to ground.

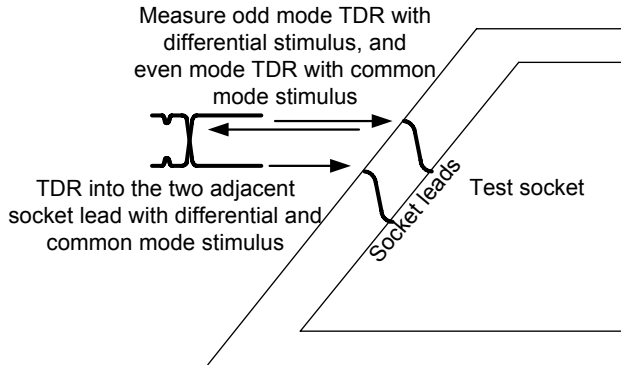

Figure 10. Measurement setup for differential TDR characterization of an ATE socket

This is why an alternative procedure using a differential TDR modeling approach discussed in [5] can be applied, which does require a short connection on the inside of the socket. In this alternative procedure, a differential (odd) and a common (even) mode TDR are used to compute the full L and C matrices for a pair of the adjacent socket leads directly, immediately providing the self and mutual parasitics information.

The equations for computing self and mutual parasitics are based on the even and odd mode impedance profiles, and are as follows:

$$L_{self} = \frac{1}{2}(Z_{even} t_{even} + Z_{odd} t_{odd}) \quad (8)$$

$$L_m = \frac{1}{2}(Z_{even} t_{even} - Z_{odd} t_{odd}) \quad (9)$$

$$C_{tot} = \frac{1}{2}\left(\frac{t_{odd}}{Z_{odd}} + \frac{t_{even}}{Z_{even}}\right) \quad (10)$$

$$C_m = \frac{1}{2}\left(\frac{t_{odd}}{Z_{odd}} - \frac{t_{even}}{Z_{even}}\right) \quad (11)$$

where C_{tot} is the total socket lead capacitance, $C_{tot} = C_{self} + C_m$. This approach assumes that the socket leads under test are symmetric, which is true for most ATE sockets. To achieve good characterization accuracy, the board traces leading to the socket leads under test must be symmetric as well. The differential approach may a more practical way for characterizing socket parasitics when the fixturing recommended in [6] for inductance characterization may not be readily achieved. The differential modeling capability and even-odd impedance profile analysis of IConnect software allows the test engineer to perform computations in equations (8)-(11) very easily [5].

It should be noted that in order to yield an even impedance profile, the test engineer needs to perform a common mode TDR measurement. Such a measurement requires the engineer to provide a good ground plane for the measurement setup, and does not allow him or her to take full advantage of the virtual ground plane effect that differential TDR measurement creates.

Differential techniques: adjacent-opposite analysis

Additionally, an “adjacent-opposite” differential technique can be applied for determining the socket self and mutual inductances. This technique is based

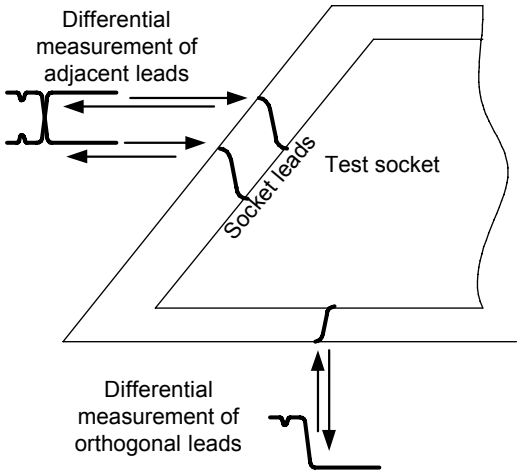

Figure 11. Measurement setup for differential TDR characterization of an ATE socket using orthogonal differential analysis technique

purely on performing two differential measurements. Thus, the test engineer can take full advantage of the virtual ground plane effect in differential TDR measurement, and does not have to provide a clean ground plane for the measurement setup. The leads on the inside of the socket do not have to be connected to ground; however, the leads under test should be connected together to achieve good measurement accuracy.

The technique is based on performing two differential measurements. In both cases, however, it is best if the leads of the socket under test are connected together. One measurement is performed on the test socket leads that are adjacent to each other and, therefore, should have some amount of mutual inductance. Using the self inductance computation procedure and equation (6), one can determine the total inductance $L_{total\ adjacent}$, which in case of such differential measurement setup will be equal to:

$$L_{total\ adjacent} = L_{self} - L_{mutual} \qquad (12)$$

The second measurement is performed on the leads which are are located far away from each other, preferably on the opposite sides of the socket (hence the name “opposite”), or on the sides which are orthogonal to each other.

This measurement is governed by the same equation (12); however, there is no mutual inductance between these leads, and therefore we can directly obtain the self inductance L_{self}.

$$L_{self} = L_{total\ opposite} \qquad (13)$$

Then, L_{mutual} can be determined as

$$L_{mutual} = L_{total\ opposite} - L_{total\ adjacent} \qquad (14)$$

This technique primarily applies to inductance measurements. In order to obtain self capacitance, the engineer can apply single-ended TDR techniques discussed above.

Bibliography

[1] M.D. Tilden, "Measuring controlled-impedance boards with TDR," – Printed Circuit Fabrication, February 1992, Tektronix Application Note 85W-8531-0

[2] *TDR Theory*, Hewlett-Packard Application Note 1304-2, November 1998

[3] L.A. Hayden, V.K. Tripathi, "Characterization and modeling of multiple line interconnections from TDR measurements," – IEEE Transactions on Microwave Theory and Techniques, Vol. 42, September 1994, pp.1737-1743

[4] D. A. Smolyansky, S. D. Corey, "Printed Circuit Board Interconnect Characterization from TDR Measurements" – Printed Circuit Design Magazine, May 1999, pp. 18-26 (TDA Systems Application Note PCBD-0699)

[5] D. A. Smolyansky, S. D. Corey, "Characterization of Differential Interconnects from Time Domain Reflectometry Measurements," – Microwave Journal, Vol. 43, No. 3, pp. 68-80 (TDA Systems application note DIFF-1099)

[6] *Guideline for Measurement of Electronic Package Inductance and Capacitance Model Parameters*, – JEDEC Publication #123, JC-15 Committee, October 1995

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