Application Note

Disk Drive Flexible Interconnect Characterization Using TDR

Introduction

Increased demands on the disk drive industry for higher performance, data throughput, and speed have resulted in a transition from the use of twisted pair interconnect to flexible board interconnect, to connect disk drive read/write heads and the pre-amplifier. The flexible board interconnect provides better mechanical properties and electrical impedance control, while creating new possibilities for placing the pre-amplifier closer to the disk drive head, which overall provides a logical path for achieving a higher data throughput for the industry.

With increasing data rates and signal rise times, the need for signal integrity SPICE and IBIS-type simulations of the signal propagation through the flexible interconnect in the disk drives has increased. The needs for disk drive interconnect characterization and equivalent circuit model accuracy have increased accordingly.

Performing the measurement: TDR instrument and probing

Because the disk drive flexible board interconnects are run differentially, differential TDR techniques are preferred for obtaining an accurate value for the interconnect impedance [1], [2]. Single-ended measurements simply do not provide complete information about the balanced signal propagation through the differential interconnect. The block diagram for the differential TDR measurement is shown in Fig. 1.

Important assumptions when doing the differential TDR measurement are:

- The lines in the Device Under Test (DUT) are symmetric. This condition is true to an acceptable degree for a typical disk drive interconnect.
- The TDR incident sources must be symmetric. This condition will always be true if a designer uses outputs of the same TDR sampling head.
- The TDR incident steps arrive at the DUT at the same time. Any skew between the TDR channels at the time TDR signals reach the DUT will result in an erroneous differential measurement and model.

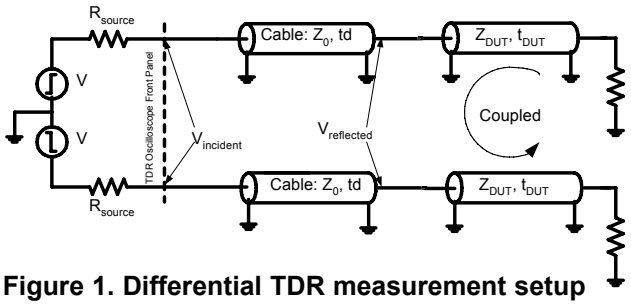

Figure 1. Differential TDR measurement setup

The last assumption implies that the measurement cables and probes interfacing the TDR instrument to the DUT must be reasonably well matched. Some small variations in cable and probe length (on the order of a few hundred picoseconds or half-an-inch to an inch in length) can be corrected for using the internal capability of TDR instruments to adjust the relative position of its step sources.

The requirement for TDR incident signals to arrive at the DUT interface at the same time also places some demands on the quality of the probes that are used in the flexible interconnect measurement, since the probes can introduce not only delays, but also asymmetric discontinuities into the measurement. Optimally, high-performance matched-length microwave probes with dual line or differential configuration should be used. As an example, the ACP-D probe from Cascade Microtech is designed specifically for dual signal contact measurements. Ground-Signal-Ground-Signal-Ground (GSGSG) configuration will ensure optimal probe performance, with Signal-Signal and Ground-Signal-Signal-Ground being acceptable for lower frequencies.

However, a simpler setup can be obtained using carefully matched coaxial probes based on semi-rigid coaxial lines with ground connections obtained using a short flexible wire soldered to the sleeve of the coax lines and then connected to the DUT grounds, where such DUT grounds are available. A short length of this wire ground connection will ensure low parasitic inductance of such probe.

If the ground connection is not available at the DUT interface point, and the closest DUT ground connection is at the far end of the flexible interconnect, a DC ground connection must still be made. Such connec-

This application note was published in Electronic Design News Magazine, June 5, 2000

tion must provide a low-inductance path between the instrument ground and the DUT ground. This low-inductance ground path can be obtained using a metal foil or wire, wrapped around or soldered to the coaxial line metal sleeve, and connected to the DUT ground plane. This metal foil DC connection must be set up so that the foil does not come in close proximity to the signal lines on the flexible board, or else the foil can become a de facto AC ground, and the AC impedance of the flexible board interconnect will be changed.

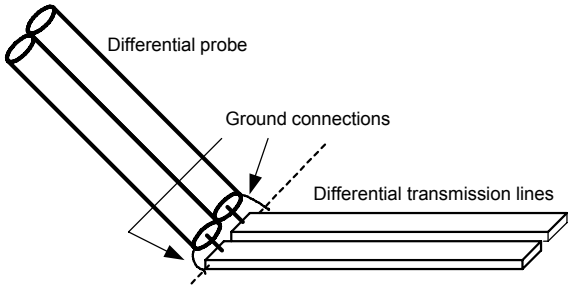

Figure 2. Practical differential TDR probe and measurement setup

In addition, it is important to note that if the suspension arm resides very close to the flexible interconnect, the suspension arm metal can effectively serve as the ground plane. Since the distance from the signal lines on the flexible board to the suspension arm may vary during the disk drive operation, this variable proximity may result in some variability of the flexible interconnect characteristic impedance. This is yet another argument for better controlling the impedance of the flexible interconnect by providing a well-defined ground plane on the back side of the flex board.

Choosing the correct model type

If a single impedance value is maintained through the interconnect length, the single TDR measurement will give the desired impedance value which can be used for the interconnect simulations. Thus, maintaining the impedance is the optimal approach from the "ease of characterization" point of view. More importantly, however, a controlled impedance interconnect will provide a much cleaner signal path and will allow the designer to propagate the signals at higher speeds without distortion, compared to the signal speeds through an interconnect that has a number of discontinuities and impedance variations.

Quite often, however, physical layout requirements dictate that the flexible interconnect trace width and, therefore, impedance, change over the interconnect length. Then a TDR instrument by itself will not give a fully accurate impedance measurement result because of the multiple reflection effects, which cause the accuracy of the instrument to deteriorate rapidly as the TDR step signal incident at the DUT propagates through multiple discontinuities in the DUT. However, an impedance deconvolution algorithm, implemented in IConnect® software from TDA Systems, allows the designer to deconvolve the multiple reflection effects and compute the true impedance profile for the DUT, providing the designer with the impedance measurement data he or she needs [3].

Based on the true impedance profile of the DUT, an equivalent SPICE model for the interconnect can be computed by IConnect software. For slow signal rise times, a lumped (RLC) model for the interconnect will suffice. A lumped model can be used when the electrical length of the interconnect is much smaller than the rise time of the signal in the disk drive system. A good rule of thumb is to ensure that the interconnect length is smaller than the signal rise time by a factor of 5 or 6:

$$t_{\text{interconnect}} < t_{rise}/6 \qquad (1)$$

The electrical length of the interconnect segment can be either measured using TDR, or evaluated using the equation below

$$t_{\text{interconnect}} = \sqrt{LC} \qquad (2)$$

where L and C are the inductance and capacitance of the interconnect segment.

For interconnect lengths comparable or longer than the signal rise time, coupled L-C segments, cascaded together, can be used. For even longer interconnects, a distributed (transmission line) model, or a combined distributed and lumped model must be used (see Fig. 3).

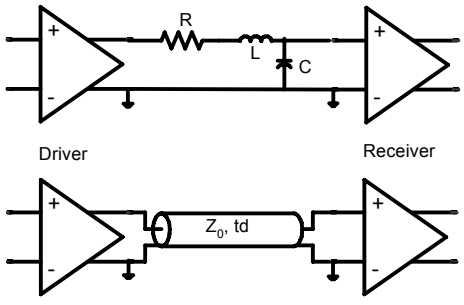

Figure 3. Single line lumped and distributed approach to interconnect modeling

For the lumped approach to work, each lumped segment should be significantly shorter than the rise time of the signal propagating through the interconnect. Lumped and distributed elements can be combined together to obtain an optimal model for the interconnect

Since the flexible interconnect is never a fully balanced structure, not only differential, but also common mode impedance needs to be determined. The ratio of common and differential mode impedances would help predict the rejection of common mode noise signals. In addition, a differential pair with both differential and common mode signals present is best analyzed as a coupled line pair. Correspondingly, the differential interconnect in disk drives, which can support both differential and common mode signals, needs to be treated as a coupled transmission line pair, which can be represented in SPICE using a lumped or a distributed approach as follows (see Fig. 4).

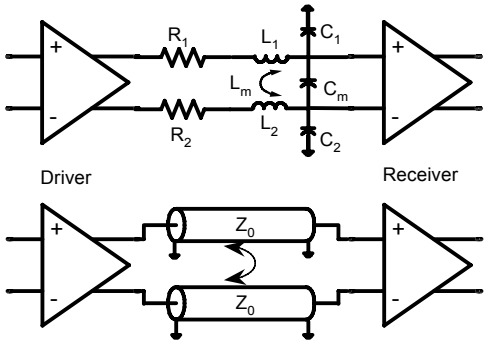

Figure 4. Differential representation of an interconnect, using a lumped or a distributed approach

In a distributed approach case, the two lines are coupled together, and the resulting coupling effects must be modeled.

The distributed coupled differential interconnect behavior has been typically modeled using multiple cascaded lumped segments. TDA Systems' application note [4] presents some more efficient approaches to modeling the differential interconnect, which are discussed below in more detail.

Modeling the flexible interconnect

As previously discussed, if the flexible board interconnect is designed to be a controlled impedance system, a TDR instrument by itself can provide an accurate impedance readout in single-ended, differential or common mode, which would allow the user to characterize the interconnect from the TDR measurements directly.

However, other restrictions are typically imposed on the flexible interconnect design and layout. As a result, a fully controlled impedance environment is difficult to achieve, and multiple discontinuities in the interconnect result in multiple reflections and signal distortion. In order to obtain a model for such flexible interconnects, the designer can follow the procedure discussed in TDA Systems' application note [3], and based on the true impedance profile computed by IConnect® software from TDA Systems, create a single or coupled line model for the interconnect. This interconnect model created by IConnect software can include several distributed or lumped model segments cascaded together.

Single line models

After the single model is created using IConnect software (based on the true impedance profile for the DUT), this model is verified using a direct interface in IConnect to a user-defined SPICE simulator[1]. As a result, the designer obtains a SPICE model that will accurately represent the interconnect behavior in his or her simulation tool. Such interconnect models are also compatible with IBIS simulation tools.

A single-line model will be valid if the common mode impedance is much higher (approximately an order of magnitude higher) than the differential mode impedance throughout the interconnect length. If this is the case, the common mode signals are fully rejected, and a simple single line model will be sufficiently accurate.

Differential models

If the differential and common mode impedance values are comparable in any segment along the interconnect length, then a more accurate model, which will accurately represent both differential and common modes of propagation in the interconnect, is required. If this is the case, designer can utilize the lumped or distributed differential line models discussed in TDA Systems' application note [4], based on even[2] and odd[3] (common and differential) impedance profile analysis. One has to keep in mind that even and odd mode analysis assumes that both conductors in the coupled line structure must be symmetric. This assumption holds very well for a typical disk drive flexible interconnect.

The corresponding distributed coupled line model, based on the even and odd impedance profiles, can be represented by the circuit diagram shown on Figure 5, reference [4].

The even and odd impedances for the distributed model can be obtained by performing an impedance profile computation on the differential and common mode TDR waveforms.

[1] Please refer to IConnect product brochures for information on currently supported SPICE simulators

[2] Even mode impedance: impedance of a single line in a coupled line pair when the two lines are driven with a common mode signal

[3] Odd mode impedance: impedance of a single line in a coupled line pair when the two lines are driven with a differential signal

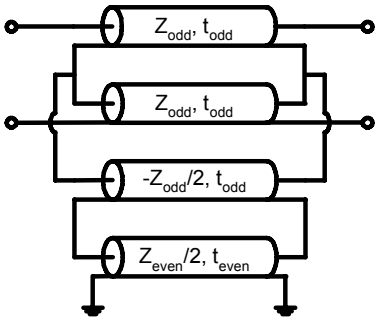

Figure 5. Differential pair model based on the even and odd impedance and delay values

Some SPICE simulators will not accept negative impedance values. In order to ensure generality of the distributed SPICE model in Fig. 5, the actual representation of this model, as extracted by IConnect software, will appear as shown in Fig. 6.

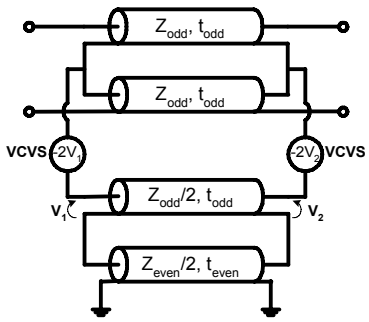

Figure 6. Practical implementation of the symmetric coupled line model by IConnect software

The voltage controlled voltage sources (VCVSs) are used to effectively present negative impedance required by the mathematical description of this model. The transmission line and VCVS model implementation will ensure that any generic SPICE or IBIS simulator can easily simulate this distributed model.

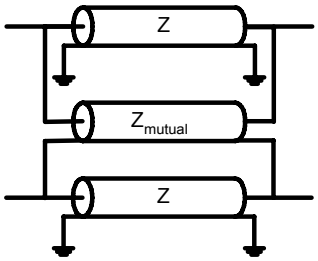

Figure 7. Simplified differential transmission line model

In addition, a simplified distributed model for the differential pair in the flexible interconnect can be used if one can neglect the differences between the even and odd mode delays. Most of the time, this assumption is not true, but for the sake of simplicity, a designer may choose the 3-line distributed model shown in Fig. 7.

Here, $Z=Z_{even}$, and Z_{mutual} can be found as

$$Z_{mutual} = \frac{2 \cdot Z_{odd} \cdot Z_{even}}{Z_{even} - Z_{odd}} \qquad (3)$$

This 3-line model will still be accurate if the differential mode impedance is significantly lower than the common mode impedance of the disk drive flexible differential interconnect. If this is the case, common mode signals essentially can not propagate, and common mode delay and impedance can be mostly ignored, as the model simplifies to the single line model shown in Fig. 3.

If a lumped approximation for the interconnect segment can be applied, the lumped differential model element values can be computed from the even and odd mode analysis as well, using the following equations:

$$L_{self} = \left(Z_{even} t_{even} + Z_{odd} t_{odd}\right)$$

$$L_{mutual} = \left(Z_{even} t_{even} - Z_{odd} t_{odd}\right)$$

$$C_{total} = \left(\frac{t_{odd}}{Z_{odd}} + \frac{t_{even}}{Z_{even}}\right) \qquad (4)$$

$$C_{mutual} = \left(\frac{t_{odd}}{Z_{odd}} - \frac{t_{even}}{Z_{even}}\right)$$

where $C_{total} = C_{self} + C_{mutual}$

Model frequency range of validity

The 3dB equivalent frequency range of validity for any given model can be computed based on the real driver rise time using the following approximate equation:

$$f_{3dB} = 0.35 / t_{rise} \qquad (5)$$

To obtain an accurate interconnect model, it is important to make sure that the model is validated up to the given specified driver rise time. In addition, attempting to create a model that works up to the frequencies and rise times that are much higher and faster than those determined by the system driver may result in a model that is unnecessarily complex and takes too much time to develop.

Example of disk drive flexible interconnect modeling session

IConnect® interconnect modeling methodology has been discussed in more detail in the application note [3]. It flows through the Measure -> Model -> Simulate and Verify path, which we will follow here for modeling of a flexible interconnect used in a disk drive.

The coaxial probing approach discussed in the section "Performing the measurement: TDR instrument and probing" is utilized in this example. The TDR stimulus is applied at the Read/Write head side of the flexible board interconnect. The flexible board is not metal plated, and the closest ground connection is at the far end of interconnect, which is attached to the disk drive pre-amplifier. The pre-amplifier input resistance is modeled as part of the overall interconnect model.

The first step is to acquire the even and odd mode TDR waveforms. The odd mode waveform is observed on Channel 1 while the TDR channels are put in differential mode. Correspondingly, an even mode waveform is observed on Channel 1 while the TDR channels are in common mode. The reference step waveform, required for computing the true DUT impedance profile, is acquired by shorting the ends of the probes together to ground.

Because of the complexity of the interconnect layout, we cannot determine the impedance of the flexible interconnect from the TDR measurement alone (see Fig. 8). However, the impedance profile waveforms, computed in IConnect software, provide much more meaningful information about the impedance and delays in the flexible board interconnect. In addition, the waveforms serve as a starting point for the interconnect equivalent circuit model extraction (see Fig. 9). Note that switching the TDR scope into the "ρ" (reflection coefficient) or "Z" (impedance) measurement mode, or using the normalization, will not give the same impedance readout, because neither approach takes into account the multiple reflection effects *inside* the DUT.

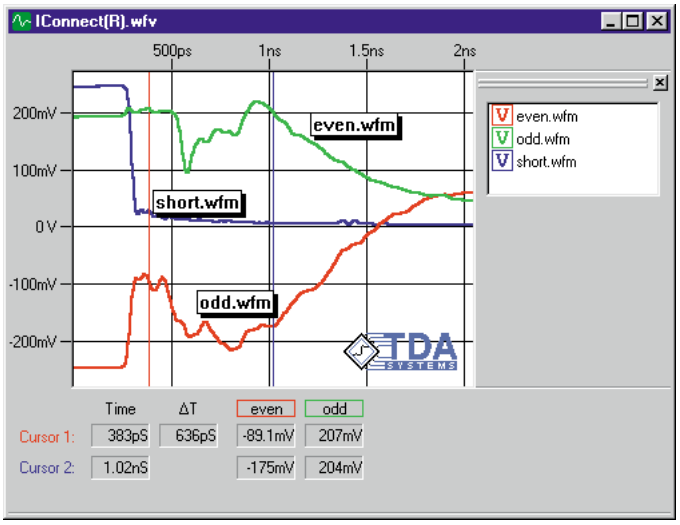

Figure 8. TDR data of the hard disk drive flexible interconnect

In Fig. 8, the short reference waveform is acquired in order to define the DUT measurement reference plane and to compute the true impedance profile for the interconnect.

As shown in Fig. 9, the characteristics of the flexible board interconnect, such as impedance and delay, can be observed much more readily.

Once the even and odd impedance profiles are obtained, the equivalent circuit model can be computed using the IConnect Symmetric-Coupled line-modeling window (see Fig. 10).

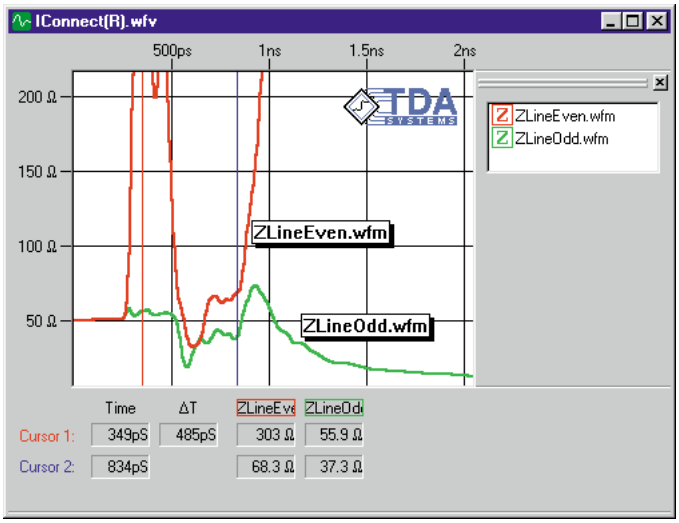

Figure 9. Even and odd impedance profiles computed from the TDR data

The solid and dashed lines of Fig. 10 determine the position of the even and odd mode delays, correspondingly, for each model segment. The parameters for the selected (blue) segment are displayed to the right of the window. Partial SPICE listing of this model computed by IConnect is given in the Appendix.

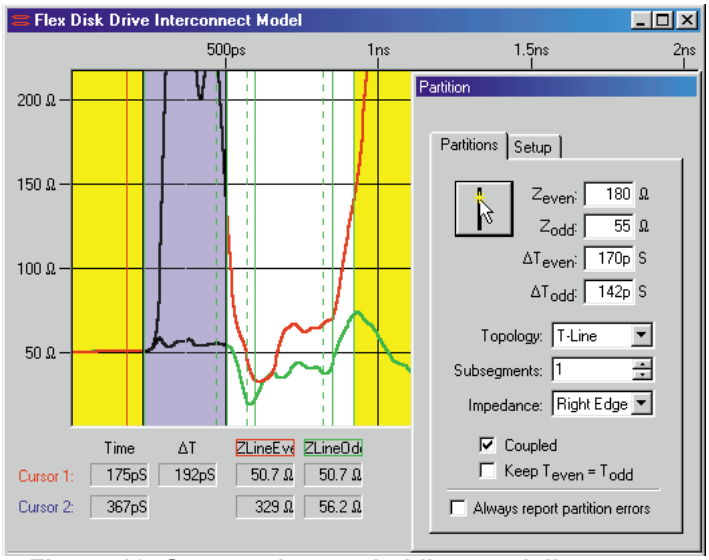

Figure 10. Symmetric-coupled line modeling window

In order to avoid excessive complexity of the model, it is important at this point to make an assumption about the device rise time and the frequency range of validity of the model. We assume 200ps to be the device rise time, which should result in a model that is neither overly simplistic nor excessively complex, and has the 3dB frequency range of validity of approximately1.5-1.8Ghz (see equation 5). With this assumption, any segment of 30-50ps or less can be considered lumped, and any segment longer than

that should remain a transmission line. Therefore, the first and third segments in Fig. 10 (each one on the order of 150ps), are modeled using transmission line elements, whereas the second and fourth segments (each one on the order of 30-40ps), are modeled as a lumped component. The input pre-amplifier resistance is shown to be 14 Ohms.

Next, the device model is complemented with the piecewise-linear SPICE model for the TDR source, and the overall system is simulated with even and odd mode simulation stimuli. The resulting simulation is compared to the measurement in the IConnect waveform viewer (see Fig. 11).

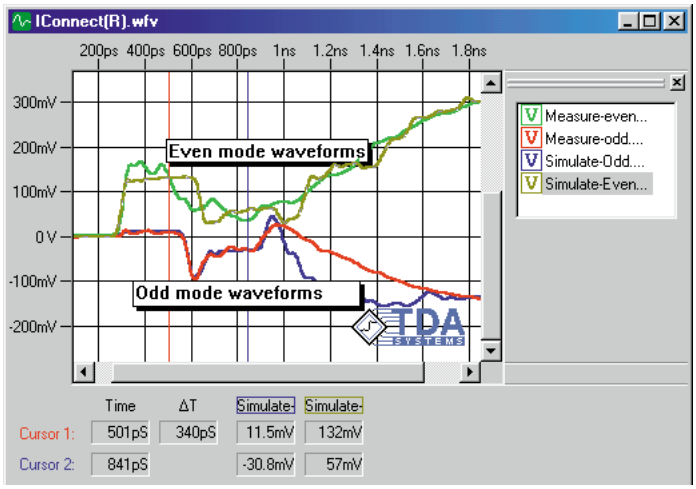

Figure 11. Comparison of simulated and measured waveforms, performed at full TDR oscilloscope rise time

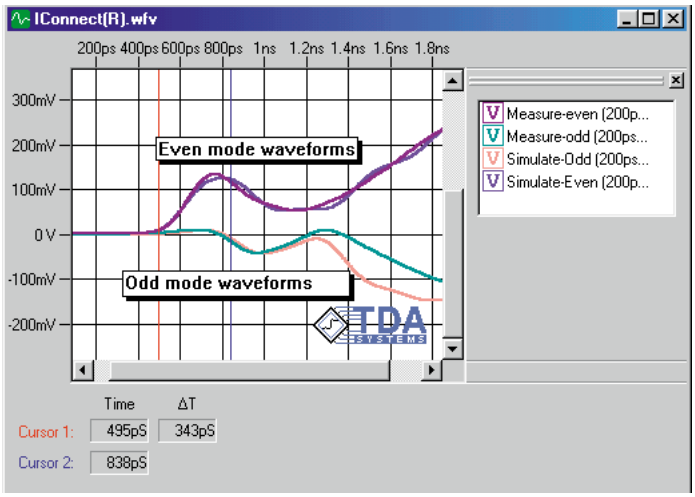

Figure 12. Correlation is improved when comparison between the simulation and measurement is performed at the device-specific 200ps rise time

At the full TDR oscilloscope rise time of 30-40ps, the correlation is not perfect; however, as we discussed previously, the target device rise time was assumed to be 200ps. Having filtered the simulated and measured waveforms at that rise time, we obtain a much closer correlation between simulation and measurement, which confirms the overall accuracy of the model at the target device rise time and desired frequency range of validity.

Conclusions

We have demonstrated a methodology for obtaining an optimal equivalent circuit model for flexible interconnect in the disk drive read/write head interface to the pre-amplifier electronics. This methodology is based on TDR measurements of the interconnect system, and provides interconnect models that can be used with any SPICE or IBIS simulation tool.

Appendix I

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* Time Domain Analysis Systems. Automatically Generated
.subckt Flex_Disk_Drive_Interconnect_Model p1 p2 p3 p4 gnd_
****** Partition #1
  t1  port1  1  2  3 Z0=55 TD=142p
  t2  port3  1  4  3 Z0=55 TD=142p
  e1  5  1  5  6 2
  e2  7  3  7  8 2
  t3  5  6  7  8 Z0=27.5 TD=142p
  t4  6  gnd_  8  gnd_ Z0=90 TD=170p
****** Partition #2
  l1  2  9 1.13n
  c1  9  gnd_ 1.38p
  l2  4  10 1.13n
  c2  10  gnd_ 1.38p
  c3  9  10 126f
  k1 l1 l2 382m
.ends
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Bibliography

[1] "Differential Ohms Measurement with the 11800-Series Oscilloscope," - Tektronix Technical Brief 47W-7520

[2] M.M. McTigue, C.P. Duff, "Differential Time-Domain Reflectometry Module for a Digital Oscilloscope and Communications Analyzer," - Hewlett-Packard Journal, December 1996

[3] "PCB Interconnect Characterization from TDR Measurements" - TDA Systems Application Note PCBD-0699

[4] "Characterization of Differential Interconnects from TDR Measurements" - TDA Systems Application Note DIFF-1199

11140 SW Barbur Blvd., Suite 100, Portland, OR 97219, USA
Telephone: (503) 246-2272 Fax: (503) 246-2282
E-mail: info@tdasystems.com Web site: www.tdasystems.com
The Interconnect Modeling Company™