Application Note

Ensuring Signal Integrity in Microprocessor Motherboards and Memory Modules

TDR and Frequency Domain Analysis Can Do the Trick

Introduction

As the speeds of interface busses between the PC microprocessor and the memory go up, these busses begin to pose some unique design challenges for a digital designer. These challenges include increased signal reflections, crosstalk, and losses that must be analyzed and understood in order for a memory system to function properly.

IBIS and SPICE simulations of microprocessor chipsets and memory systems are necessary to ensure that the signal propagates through the computer motherboard with minimal distortion, without causing erroneous switching patterns and signal degradation — ensuring the signal integrity in the motherboard design. The accuracy of such simulation depends completely on the accuracy of the models for the interconnect components of the digital design, such as board traces, connectors and packages. The accuracy of these models can be ensured with the use of TDR instrumentation, a very easy-to-use and intuitive technology for obtaining accurate models for the digital system components [1].

TDR Measurements

The TDR oscilloscope is widely used for signal integrity and interconnect characterization work. Its wide acceptance is due to the fact that it is a very visual and intuitive technology, and the TDR waveform can be relatively easily correlated to the physical structure of the interconnect (Figure 1).

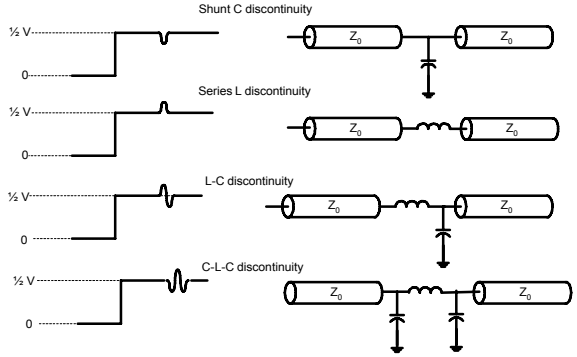

Figure 1. TDR waveform features can be easily correlated to the physical structure of the interconnect

When performing a TDR measurement, a designer must deal with the multiple reflections in a TDR waveform. These multiple reflections can significantly distort the picture that an instrument presents to the designer if the Device Under Test (DUT) consists of several layers of impedance, usually the case for a typical computer motherboard. However, an impedance deconvolution algorithm, implemented in TDA Systems' IConnect® TDR software, can be applied to compute the DUT true impedance profile and minimize the multiple reflection effects ([2], Figure 2).

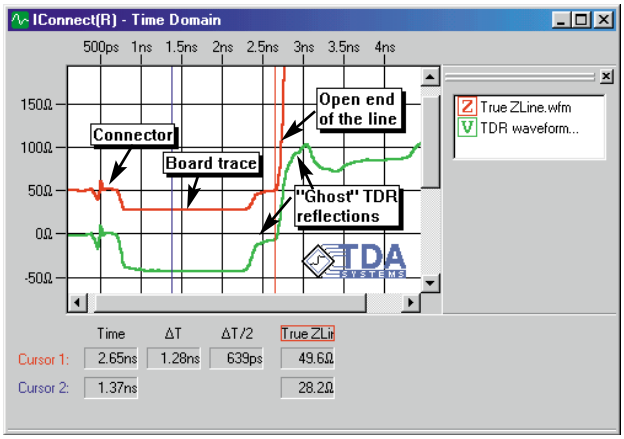

Figure 2. True impedance profile, computed from TDR data in IConnect® TDR software, minimizes the multiple reflection effects and enables easy correlation between the TDR trace and the physical structure of the DUT

In this figure, the true impedance profile removes the multiple reflections that may confound the designer, who is analyzing the DUT using the TDR instrumentation. The true impedance profile, then, enables the designer to quickly correlate the capacitance and inductance (CL) segment in the beginning of the waveform on Figure 2 to the board-level connector, and the straight impedance segments in the middle to the board traces with different impedances.

Modeling the PC Motherboard

The true impedance profile provides a solid basis for modeling the processor-to-memory interface. The models that we extract based on the true impedance profile must be sufficiently accurate to

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predict the potential signal integrity issues with the fast digital signals propagating through the mother-board.

Since we know qualitatively how the true impedance profile waveform correlates to the transmission line and lumped models, we can quickly partition the true impedance profile waveform and compute the model. The transmission line segments, which in the true impedance profile waveform are represented by straight line sections, are modeled using T-line elements of appropriate impedance and delay. When computing the model by hand, keep in mind that the delay provided by the impedance profile is the round trip delay. This means you must divide the delay by two to get an accurate model. The lumped component values can be computed using the following equations:

$$C = \frac{1}{2}\cdot\int_{t_1}^{t_2}\frac{1}{Z(t)}dt \qquad L = \frac{1}{2}\cdot\int_{t_1}^{t_2} Z(t)dt \tag{1}$$

where t_1 and t_2 are the boundaries of the lumped segment. IConnect TDR software uses the true impedance profile, which it computes beforehand, to compute the appropriate Z, t_d, L and C values automatically.

Sometimes, a lumped model is appropriate for the application even when it appears that a transmission line model is required. For slow signal rise times, a lumped (RLC) model for the interconnect may suffice. A lumped model can be used when the electrical length of the interconnect is much smaller than the rise time of the signal in the system. A good rule of thumb is to ensure that the interconnect length is smaller than the signal rise time by a factor of 5 or 6:

$$t_{\text{interconnect}} < t_{rise}/6 \tag{2}$$

A sample SPICE listing, extracted in IConnect, is shown below. The impedance profile waveform on figure 3 is partitioned into segments, each of them representing a transmission line impedance section. Appropriate lumped or distributed topologies can be selected using Figure 1 and 3 as a guideline.

Sample SPICE Model Listing Generated by IConnect TDR Software

```
.subckt Memory_Trace_Model port1 port2 gnd_
****** Partition #1
  t1  port1  gnd_  1  gnd_ Z0=49.9 TD=325p
****** Partition #2
  t2  1  gnd_  2  gnd_ Z0=27.4 TD=273p
****** Partition #3
  t3  2  gnd_  3  gnd_ Z0=40.5 TD=645p
****** Partition #4
  t4  3  gnd_  port2  gnd_ Z0=27 TD=273p
.ends
```

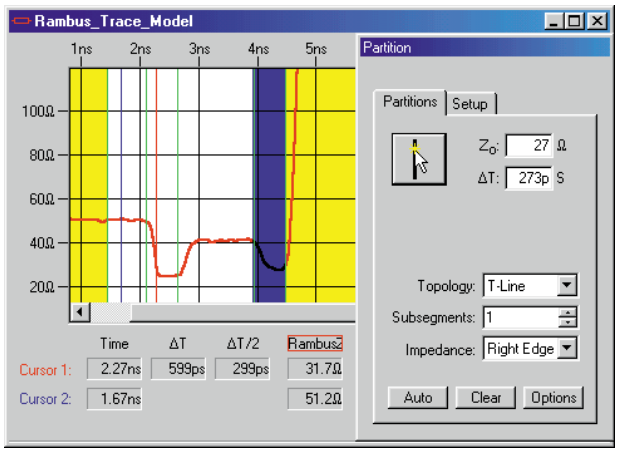

Figure 3. Create a model for the memory module based on the true impedance profile. This model will accurately predict reflections and ringing in the module

Once the model for the memory module has been generated, it is important to validate the model by comparing its simulation to the real measurement again. This step is required in order to validate the model and to ensure that the true impedance profile was partitioned into segments accurately, and that the appropriate lumped or distributed topology was selected for each segment.

IConnect TDR software comes in handy when recreating the model for the TDR source, which is important to properly correlate the simulation of the extracted model to the TDR measurements. In addition, it is important to validate the model using a rise time that corresponds to the real device rise time. Using the TDR instrument rise time of about 35 ps may result in models that are excessively complex for the application and take too much time to develop. For the Rambus module, we should select a 100 ps rise time or slower for validation purposes. The resulting comparison (Figure 4) is

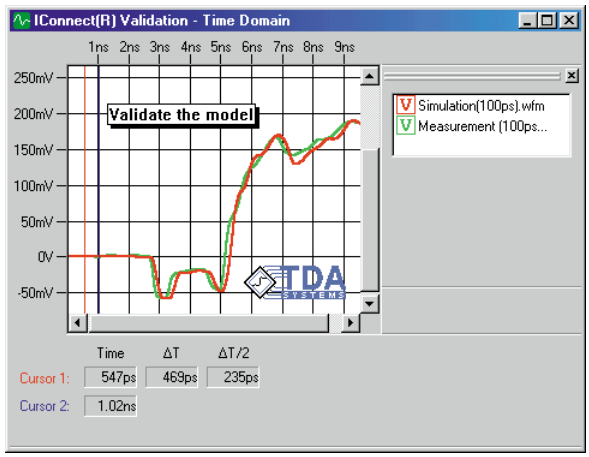

Figure 4. Validate the model at the real device rise time. Using the TDR oscilloscope rise time of 35 ps may result in models that are too complex for the application and take too much time to develop

generated using the interface between SPICE simulations and measurements in IConnect TDR software.

Additionally, models for differential clock lines in Rambus memory module can be extracted, as discussed in [3]. However, since the differential clock lines in Rambus memory modules are typically not laid out to couple tightly, a single line model for these lines will suffice. A differential, or coupled line, model discussed in [3] can also be used to characterize crosstalk and coupling between the lines. This differential line model, combined with loss characteristics of the line, will accurately predict interconnect-induced jitter and eye diagram.

Modeling Input Die and Package Capacitance

Input capacitance of the die can be used to load the Rambus memory module traces and effectively decrease their impedance to provide a complete matched impedance path. For that reason, knowing the input die and package capacitance can be important. JEDEC and IBIS standards [4], [5] provide guidelines for computing the package parasitics as well as input die capacitance. For example, computing the package and die capacitance involves making a TDR measurement into the package lead through a fixture, and then making a TDR measurement through the fixture but without the packaged part inside. The integral of the difference between the two waveforms asymptotically gives you the overall capacitance value (Figure 5).

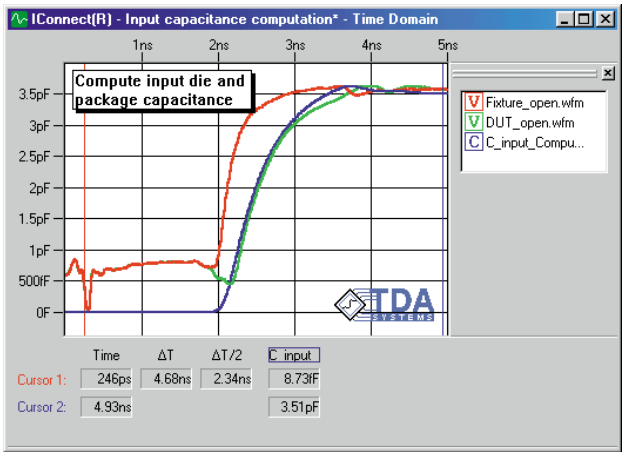

Figure 5. Compute input die and package capacitance from the TDR analysis. The capacitive value in this example is estimated to be 3.5 pF

As we pointed out before, it is the asymptotic capacitance value that we are after. Having read the value at the end of the computed capacitance waveform, we obtain a value of 3.5 pF for our input die and package capacitance.

Spectrum and S-parameters

Further analysis of the TDR data for the memory module can be performed in IConnect TDR software using its spectrum and S-parameter computational capabilities. Let's consider the simulated and measured data, which we analyzed in Figure 4. In Figure 6, the comparison of the spectra for the measured and simulated waveform for the memory module exhibits good correlation up to about 2.2 GHz, above which frequency we can see some discrepancy. This discrepancy in frequency domain, however, does not cause significant discrepancy in the time domain data. We can still consider 35 ps rise time and the 3 dB bandwidth of 10 GHz, corresponding to that rise time, as the range of validity for the model of this digital interconnect.

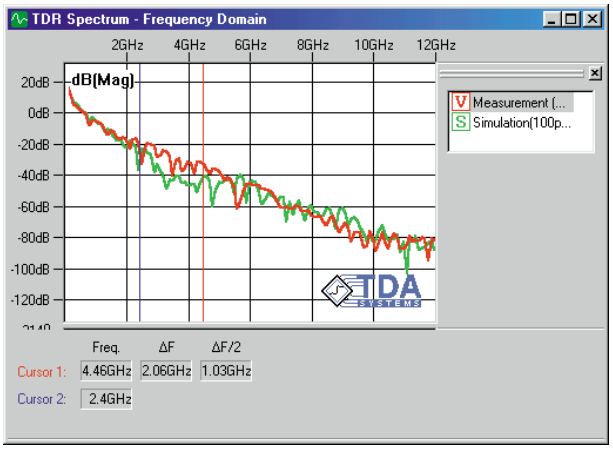

Figure 6. Spectrum of the simulated and measured TDR waveforms. S-parameters for the DUT can be computed just as readily in IConnect TDR software

Remember that the spectrum is not representative of the losses in the interconnects, but the S-parameters for the given interconnect are. S-parameters for the DUT can be computed in IConnect TDR software using the TDR data for the DUT and the reference open TDR waveform, which can be obtained by disconnecting your probe from the DUT and performing a TDR measurement into the open air.

The following graph (Figure 7) is the S11 computation based on the memory module TDR data. It should be noted that the losses, exhibited by the memory module trace, are only partly due to the actual loss mechanisms in the board itself, such as skin effect and dielectric loss. This measurement also includes the losses due to reflection of the signal at the impedance discontinuities in the memory module. Therefore, in this measurement the board losses are superimposed with what is referred to as "reflection loss," or the amount of signal reflected back to the source from the transmission line discontinuities, to create a complete return or insertion loss picture.

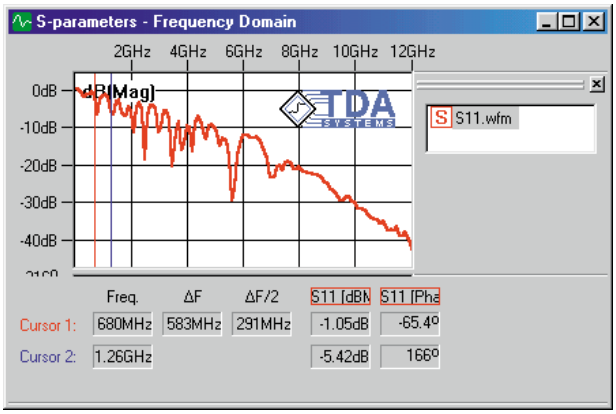

Figure 7. S11 for memory module trace computed in IConnect from TDR measurement. This measurement exaggerates the board losses because it adds the actual board losses and the losses due to reflection of the signal from the board discontinuities

In order to characterize the actual losses in the board, the designer has to measure the Time Domain Transmission (TDT) on controlled impedance board coupons. The following example shows a measurement of a controlled impedance board coupon of about the same length as a typical memory module trace, both laid out on an FR4 substrate. The resulting S21 transmission data for this coupon is displayed in Figure 8.

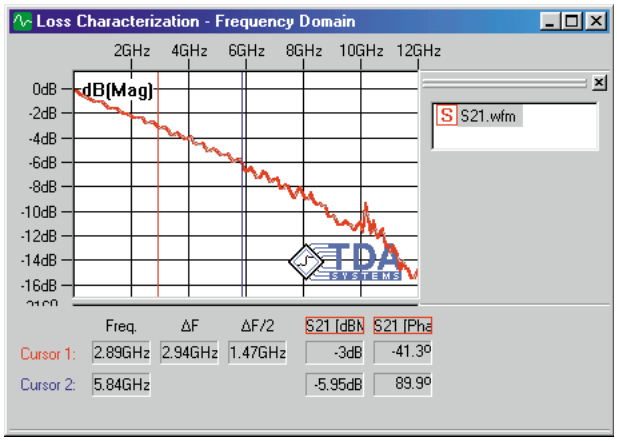

Figure 8. S21 computed from TDT measurement

This figure demonstrates that the actual 3 dB bandwidth for this coupon is about 2.9 Ghz. The 3 dB bandwidth is representative of the losses in the structure because it shows the bandwidth at which the signal amplitude will decrease by exactly one half.

Additionally, differential and mixed mode S-parameters can be computed in IConnect TDR software to help with characterization of differential transmission lines. For example, differential S-parameters can be used to characterize the crosstalk between the differential pairs. The mixed port S-parameters can be obtained by exciting the circuit with a differential mode stimulus and analyzing the common mode response at the ports.

When computing S-parameters, the designer must also keep in mind that 40-50 dB is about the maximum dynamic range that the TDR oscilloscope measurement can provide under normal operating conditions. The dynamic range of 40 dB, however, is more than adequate for high-speed digital interconnect characterization. Additional calibration techniques may be applied to increase the dynamic range of the TDR oscilloscope [6] and achieve dynamic range in frequency domain that is comparable to the dynamic range of vector network analyzers.

Conclusions

We have demonstrated a methodology for obtaining an optimal equivalent circuit model for interconnects in the memory module and some of its components. This methodology is based on TDR measurements of the interconnect system, and provides interconnect models that can be used with SPICE or IBIS simulation tools to predict reflections, ringing and crosstalk in memory systems. Additionally, frequency domain spectrum and S-parameter data computed from TDR measurement with the aid of IConnect TDR software provide information about frequency range of validity and losses in the digital system.

Bibliography

[1] M.J. Resso, B. Chia, "Accurate Measurements On High-Speed Rambus Traces Present Challenges," – Electronic Design, March 20, 2000
[2] Smolyansky, Corey, "PCB Interconnect Characterization from TDR Measurements" – TDA Systems Application Note PCBD-0699-02, published in Printed Circuit Design Magazine, May 1999
[3] Smolyansky, Corey, "Characterization of Differential Interconnects from TDR Measurements" – TDA Systems Application Note DIFF-1199, published in Microwave Journal, March 2000
[4] "Guidelines for Measurement of Electronic Package Inductance and Capacitance Model Parameters," – JEDEC Publications JEP-123,
[5] "I/O Buffer Accuracy Handbook," – EIA IBIS, Revision 2.0, April 20, 2000
[6] L.A. Hayden, V.K. Tripathi, "Calibration Methods for Time Domain Network Analysis," – IEEE Transactions on Microwave Theory and Techniques, Vol 41, No. 3, March 1993, pp. 415-421

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