PCB Interconnect Characterization from TDR Measurements

Introduction

As the performance requirements for modern computer and communications systems grows, the demand for high speed Printed Circuit Boards (PCB) increases as well. Speeds as fast as 1Gbit/sec are expected to be supported by standard PCB technologies, with the rise times of these signals being as fast as 100ps. At these speeds, interconnections on PCBs behave as distributed elements, or transmission lines, and reflections due to impedance mismatch are a typical signal integrity problem that board designers encounter in their work. Vias between layers and connectors on a board create discontinuities that distort the signals even further. To accurately predict the propagation of the signals on a board, designers need to determine the impedance of their traces on different layers and extract the models for board discontinuities.

Time Domain Reflectometry (TDR) measurements have always been the measurement approach of choice for board characterization work [1], [2]. Based on TDR measurements, a circuit board designer can determine characteristic impedances of board traces, compute accurate models for board components, and predict board performance more accurately.

## PCB trace impedance profile computation

TDR oscilloscope basics

In a simple TDR setup, shown on Figure 1, incident waveform amplitude at the Device Under Test (DUT) is typically half the original stimulus amplitude V at the TDR source. The smaller DUT incident waveform amplitude is due to the resistive divider effect between the 50 Ω resistance of the source and 50 Ω impedance of the coaxial cables connecting the TDR sampling head and the DUT. The impedance of the board trace can be determined from the waveform measured by the TDR oscilloscope, $V_{measured}$, which is the superposition of the incident waveform at the DUT and the reflected one, offset by 2 electrical lengths of the cable interconnecting the oscilloscope TDR sampling head to the DUT.

Traditionally, the impedance of the board is computed from TDR measurements using an equation that relates the DUT impedance to the impedance of the cable interconnecting the TDR oscilloscope sampling head to the DUT:

$$Z_{DUT} = Z_0 \cdot \frac{1+\rho}{1-\rho} \qquad (1)$$

where ρ is the reflection coefficient, which is a ratio
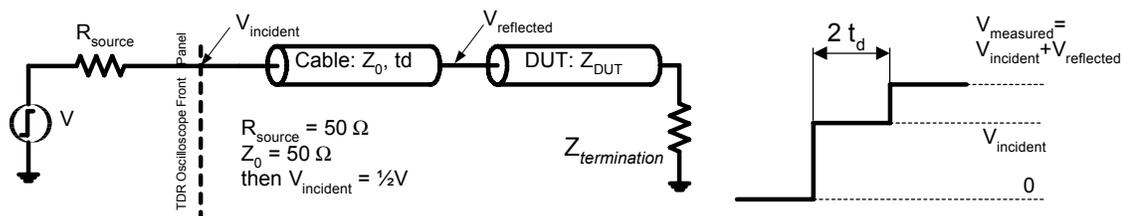
Figure 1. TDR oscilloscope equivalent circuit. The waveform reflected from the load is delayed by 2 electrical lengths of the cable interconnecting the DUT to the TDR oscilloscope, and superposed with the incident waveform at the TDR sampling head

of reflected and incident energy at the DUT:

$$\rho = \frac{V_{reflected}}{V_{incident}} \qquad (2)$$

The reflection coefficient can be computed and displayed by a TDR oscilloscope.

The equation (1) can be rewritten in terms of incident and reflected waveforms, or can include the waveform actually measured at the input of the oscilloscope TDR sampling head:

$$Z_{DUT} = Z_0 \cdot \frac{V_{incident} + V_{reflected}}{V_{incident} - V_{reflected}}$$

$$= Z_0 \cdot \frac{V_{measured}}{2 \cdot V_{incident} - V_{measured}} \qquad (3)$$

Either equation (1) or (3) can be used to compute the impedance of the DUT.

Multiple reflection effects and the impedance peeling algorithm.

For a simple DUT, such as a test coupon on a PCB, the equations above work quite well. However, in real life, a board designer has to deal with more complex structures, such as board traces that jump between layers, interconnected by vias within a board and connectors between different boards (for example, at a backplane to a daughterboard interface). Traces on different board layers can have different impedances, and vias and connectors constitute inductive and capacitive discontinuities that distort the signal propagating through a board. Such complex structures result in multiple reflections

Figure 2. Lattice diagram of TDR waveform propagating through a complex DUT with multiple impedance discontinuities. The superposition of primary reflections at each layer and multiple secondary, or "ghost," reflections between layers, makes it difficult to determine the impedance of each layer in the DUT

occurring in the system at each impedance discontinuity. The resulting superposition of real and multiple "ghost" reflections in the system makes it difficult, if not impossible, to apply equations (1) or (3) directly. The multiple-reflection effects are illustrated by the lattice diagram on Figure 2.

Even for a simple test coupon, an SMA connector that serves as an interface to the board trace can create a situation where superposition of multiple reflections results in insufficient accuracy in determination of the coupon impedance.

Computation of the true impedance profile

The true impedance profile can be computed, however, from the TDR profile measured with a TDR oscilloscope using an impedance peeling algorithm, also known as an inverse scattering algorithm [3]-[4]. From the lattice diagram on Figure 2, it is clear that equation (1) can be applied to the reflection at the interface between Z_0 and Z_1 in order to compute the impedance of layer 1:

$$Z_1 = Z_0 \cdot \frac{1 + \rho_{01}}{1 - \rho_{01}} = Z_0 \cdot \frac{V_{incident1}(1) + V_{reflected1}(1)}{V_{incident1}(1) - V_{reflected1}(1)} \qquad (4)$$
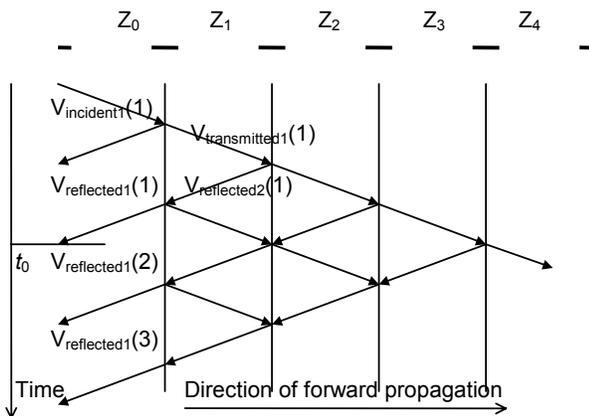
where the subscript 01 refers to reflection at the impedance discontinuity between layers 0 and 1. The reflected waveform at time t_0 is defined by the reflection between layers 1 and 2 and but also by the reflection and transmission between layers 0 and 1. The reflected waveform amplitude at time t_0 can be computed as:

$$V_{reflected}(2) = \tau_{01}^2 \cdot \rho_{12} \cdot V_{incident1}(1) + \rho_{01} \cdot V_{incident1}(2) \qquad (5)$$

where τ_{01} is the transmission coefficient at the interface between layers 0 and 1, defined as $\tau_{01} = 1 + \rho_{01}$. From this equation, ρ_{12} can be determined unambiguously, and the impedance at layer 2 can then be found using equation (1) above.

$$Z_2 = Z_1 \cdot \frac{1 + \rho_{12}}{1 - \rho_{12}} \qquad (6)$$

This computational procedure can be applied to the measured waveform, consequently peeling layers of impedance. As a result, impedance at each layer can be computed to form the true impedance profile of the DUT. The algorithm for computing the true impedance profile, often referred to as the "peeling" or "inverse scattering" algorithm, is implemented in IConnect® software from TDA Systems.

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Single line modeling

Once the impedance profile has been computed, a board designer can obtain direct readouts of impedance values for all sections of the board trace under test, or any given DUT. As an example, a 25 Ω (nominal) board trace surrounded by two 50 Ω traces has been characterized using IConnect® interconnect modeling software from TDA Systems, which implements the impedance peeling algorithm. Standard SMA connectors have been used to interface from the board to the TDR measurement system. IConnect® software computes the impedance profile based on TDR data acquired with Tektronix TDS/CSA8000, 11801/CSA803, or Agilent 86100A, 54750A/83480A and 54120 series TDR oscilloscopes.

50 Ω   25 Ω   50 Ω
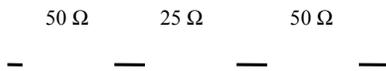
Figure 3. Test device. A 25 Ω FR4 board trace sur-rounded by two 50 Ω traces

To compute the impedance profile waveform, both the incident and reflected waveform must be known. The reflected waveform can be computed based on TDR measurements of the DUT. The incident waveform, on the other hand, can de determined in several ways. The simplest is to compute it from an acquired reference short or open waveform, where a short or an open termination is connected at the interface between the instrument cables and the DUT, in place of the DUT. A short termination typically has less reactance (an open-ended coaxial cable can have significant fringing capacitance), and is the preferred method of acquiring the reference waveform. From TDR measurements of the DUT and the reference waveform, IConnect® software will compute the true impedance profile, using the impedance peeling algorithm described above.

With multiple reflections in the TDR measurement removed, we can use the cursors in the IConnect® waveform viewer to observe the impedance of the DUT, from 50 Ω, to about 26 Ω, back to 50 Ω. The segments of constant impedance are evidently the transmission lines on the board, whereas the dips and peaks in the waveform are the capacitive and inductive discontinuities. On the true impedance profile waveform, the board designer can zoom in on the part of the DUT that needs to be modeled, without running the risk of having multiple reflection effects distort the impedance of the DUT in that

section of the trace. Unessential information, such as reflections at the connector-to-board interface, can be windowed out during the modeling session.
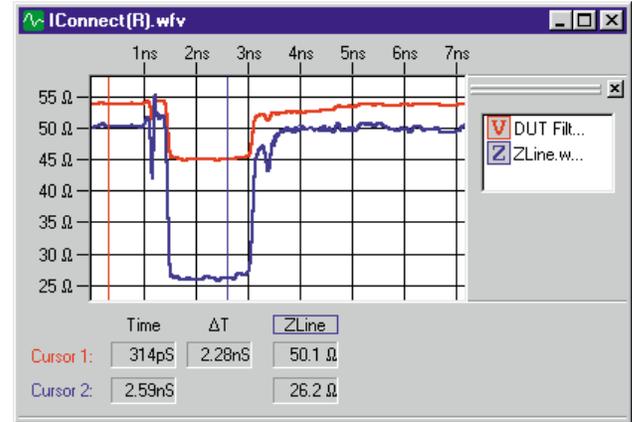

Figure 4. TDR waveform vs. the impedance profile waveform. On the impedance profile waveform, multiple reflections are removed and the true impedance values for the DUT are obtained. Waveforms are offset due to the fact that TDR waveform is in voltage vs. time scale, whereas the impedance profile waveform is in ohms vs. time

Once the engineer has segmented the impedance profile waveform, as shown Figure 5, IConnect® software automatically computes the impedances and propagation delays for the lines on the board.
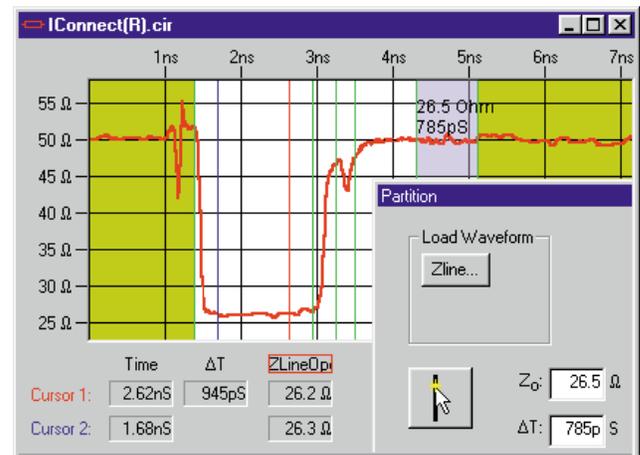
Figure 5. Connectors on the board can be windowed out to zoom in on the part of the board trace that needs to be modeled, without the risk that the multiple reflections will distort the impedance of the modeled trace. The impedance profile waveform is divided into segments which represent corresponding traces on the board. Trace impedance and electrical delay are automatically calculated by the IConnect® software

The model can then be verified using an integrated interface to SPICE. The extracted model is complemented with a piece-wise linear source that should accurately represent the TDR oscilloscope incident step waveform during the simulation, and the same termination as the one used during the measurement. Once a composite circuit is simulated, the resulting simulated waveform is compared to the measured waveform to verify the accuracy of the computed board trace impedance. This comparison, illustrated on Figure 6, clearly shows that the simulated and measured waveforms correlate well. The discontinuity due to the SMA connector at the interface to the board from the cable interconnecting the DUT with the TDR instrument is not represented in the simulated waveform, because we ignored this connector in our modeling session.
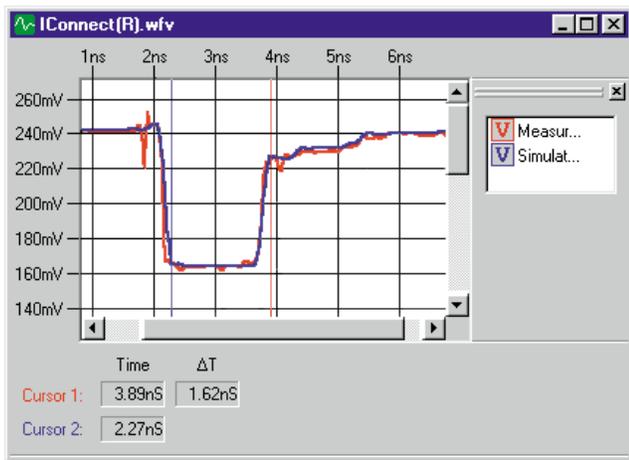
Figure 6. Comparison of simulated and measured waveform for the DUT. The SMA connector on the board was excluded from modeling and simulation session. Except for the discontinuity at the beginning of the board due to the SMA connector interface, the model represents the board trace accurately

Lumped discontinuity modeling

If required, the SMA connector on the board can be modeled as well. An inductive discontinuity will be represented on a TDR waveform as a spike above the impedance of the surrounding lines, whereas a capacitive discontinuity will be represented as a dip in the impedance profile waveform, as illustrated in Figure 7.
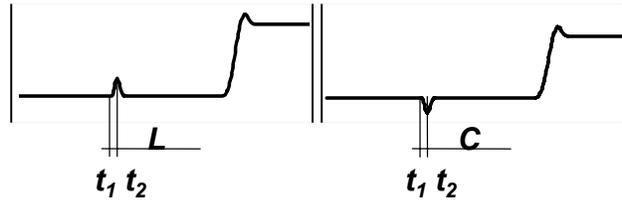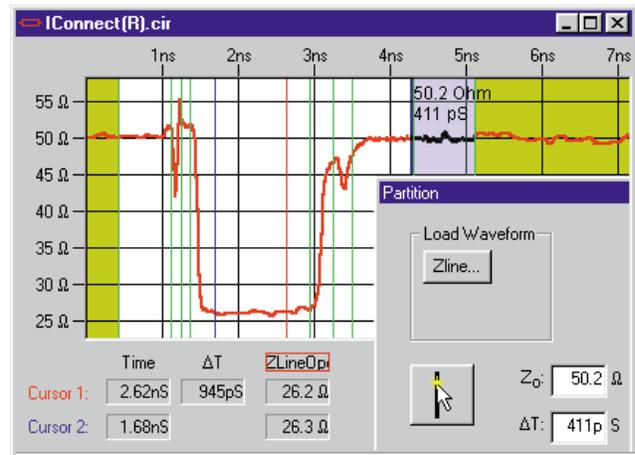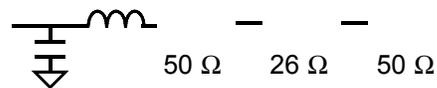

Figure 7. Inductive spike and capacitive dip on the impedance profile waveform

The corresponding values for inductance and capacitance can be computed using equations (7) [5], [6]

$$C = \frac{1}{2} \cdot \int_{t_1}^{t_2} \frac{1}{Z(t)} dt \qquad L = \frac{1}{2} \cdot \int_{t_1}^{t_2} Z(t) dt \qquad (7)$$

As an example, consider the board waveform above. As a result of modeling the connector on the board, we came up with the following model (see Figure 8).

$$50\ \Omega \qquad 26\ \Omega \qquad 50\ \Omega$$

Figure 8. Board trace model that includes modeling of the SMA type connector on the board. Connector is modeled as a shunt C — series L circuit topology

Now, once this trace has been modeled, we can again verify the accuracy of the model by simulation using the IConnect® integrated interface to PSPICE simulator. The results of the comparison can be seen on Figure 9, which shows acceptable correlation between the simulation and measurement.
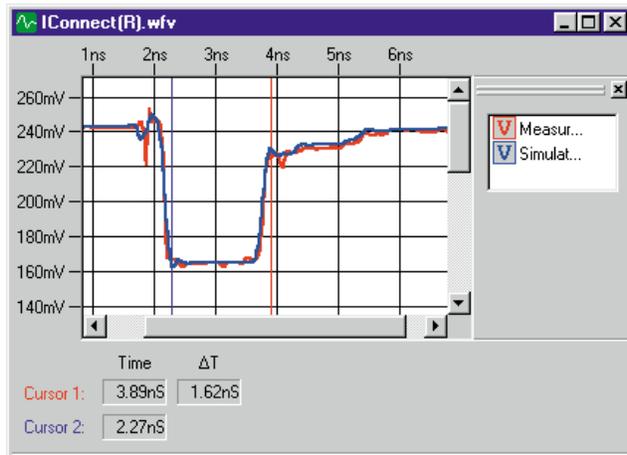
Figure 9. Comparison of simulated and measured waveform for the DUT. In addition to the board trace, the SMA connector at the DUT interface was modeled. The model represents the board trace with acceptable correlation, including the connector discontinuity

Determining the simplest model for the DUT

When doing PCB interconnect modeling, it is important to keep in mind that we need to determine a model for a board trace discontinuity that is no more complex than is necessary to represent the DUT accurately at the given system rise time or analog bandwidth.

In light of that, let us examine the relationship between the rise time of the TDR oscilloscopes to the rise time of a DUT. Typical TDR system rise time is quite fast, on the order of 30-40ps. On the other hand, even today in the world of super fast signals on the circuit board, typical rise times rarely reach 100ps, and more often are on the order of 500ps to 1ns.

With faster TDR system rise times, the DUT traces may exhibit losses that are not present under normal operating conditions for the DUT. In addition, the impedance that the lumped discontinuities present to the test signal is dependent on the highest frequency present in the test signal

bandwidth, as described by equations (8)

$$Z_C = \frac{1}{j \cdot 2\pi f \cdot C} \qquad Z_L = j \cdot 2\pi f \cdot L \qquad (8)$$

The rise time vs. analog bandwidth relationship for step-like TDR incident waveform as it is implemented in TDR oscilloscopes can be evaluated using equation (9)

$$f = \frac{0.35}{t_{rise}} \qquad (9)$$

Correspondingly, for faster rise time the capacitive discontinuity will present a deeper "dip", whereas an inductive discontinuity will be a present a larger "spike" in relation to the impedance of the transmission lines surrounding the discontinuity. Consequently, the impedance discontinuity ΔZ in the DUT will be larger for faster rise time, which may not accurately represent the impedance value at the DUT operating rise time.

At the typical TDR oscilloscope rise time of about 35 ps, the correlation between the measurement and simulation of the given model is good, but not perfect, as can be observed on Figure 9. However, once both waveforms are filtered to about 150ps equivalent rise time, the discrepancies between the model simulations and measurements become negligible. The resulting model will represent the DUT with high level of accuracy to the rise time of 150ps, as is illustrated by the Figure 10.
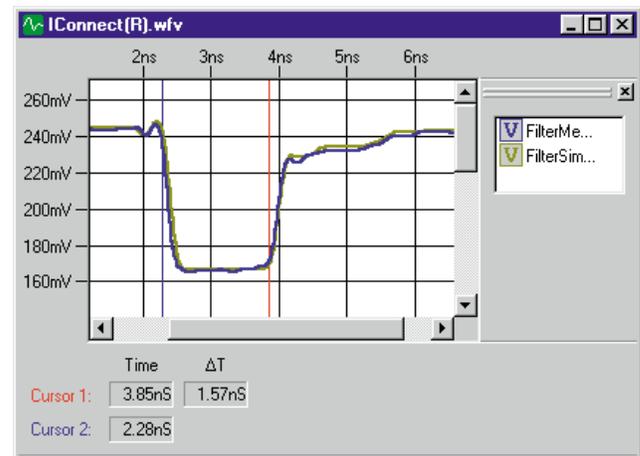
Figure 10. Comparison of simulated and measured waveforms at 150 ps rise time. Clearly, the correlation has been improved significantly at the user-defined risetime, and there is no need for further refining of extracted model

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Therefore, we can conclude that using the rise time filtering to verify the PCB trace model at the realistic device rise time will allow the engineer to characterize the DUT with a model that is simple, but adequate to represent the DUT accurately.

Conclusion

We have demonstrated a general methodology for modeling printed circuit board interconnects from TDR measurements. From the data acquired with a TDR oscilloscope, with the use of IConnect® interconnect modeling software, a circuit board designer can compute a true impedance profile for a PCB trace and accurately determine the impedance and propagation delay for a board trace running through several layers on the board. The models for lumped discontinuities, such as vias and connectors, can be computed as well, and the overall model can be verified at the user-defined rise time, using a built-in interface to a SPICE simulator. As a result, accurate models for the PCB components can be obtained more quickly, resulting in lowered design costs and faster product time-to-market.

Bibliography

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