

Direct Rambus™ Signal Integrity Measurements¹

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Biographies

Mike Resso is a Product Manager in the Lightwave Division of Hewlett Packard. He is responsible for developing technical symposiums, training seminars, and application notes for HP field engineers that will expand the worldwide market growth of signal integrity test equipment. Mike has 15 years of experience in the design and development of electro-optic test instrumentation and is the author of over 20 technical publications. He received his bachelor's degree in Electrical and Computer Engineering from University of California.

Dima Smolyansky directs Marketing and Systems Development at TDA Systems. He has been in the instrumentation and measurement industry for 7 years, working with time and frequency domain network analysis systems. He has published a number of papers and taught short courses on interconnect measurements and modeling. Mr. Smolyansky is an IEEE member since 1992. He holds the M.S.E.E. degree from Oregon State University and the Engineer Diploma (M.S.) degree from Kiev Polytechnic Institute.

Abstract

Traditional design methods fall short as the new generation of high speed computer

architectures are being developed. The need for speed drives digital edge rise times to 350 picoseconds and beyond. The design process is a new game with simple PC board traces becoming transmission lines with complex impedance. Circuit simulation models are helpful tools, but models based on discrete devices don't predict the performance actually being observed when the circuit is running. This paper will discuss measurement tools that digital designers can use to overcome these design problems and validate Direct Rambus signal integrity.

Introduction

Over the last ten years, computer processor architectures have done a remarkable job of increasing CPU performance. However, it is well known that main memory subsystems haven't kept pace with the blistering speeds of the microprocessor clocks. Although this gap has been bridged in part by improved and more sophisticated caches, data intensive images are demanding even more performance directly from the memory system. A significant development has recently changed the computer's system architecture to solve this problem.

Direct Rambus™ is a high-speed digital bus that requires circuit board traces to be impedance controlled at 28 ohms. This two byte wide bus double pumps a 400 MHz clock to enable data transfer on both the rising and falling

¹ This paper has been adapted from a paper presented at 1999 HP Users Group Meeting in San Diego, CA

clock edges. Assuming 100% utilization of the data bus, the peak bandwidth is amazing 1.6 GBytes per second.

The traditional logic analysis measurement techniques now need to be complemented with a signal integrity measurement tool. Time Domain Reflectometry (TDR) is the tool of choice for digital design engineers today.

TDR Basics

Various measurement techniques can be used to help in the design, development and troubleshooting of high-speed circuits. For evaluating the Rambus physical layer, the authors chose an intuitive method called Time Domain Reflectometry or TDR¹. Before discussing real world Rambus measurements, a brief overview of TDR fundamentals will be given. This should help the readers better understand how to interpret the TDR test data presented in this paper.

Time Domain Reflectometry is a method that utilizes a high speed digitizing oscilloscope with a built in step generator capable of launching a fast edge into a device under test (DUT). By monitoring the reflected wave from various impedance discontinuities encountered in the DUT, many characteristics of the device can be analyzed². Whether or not a component adds excess inductance or excess capacitance to the circuit is of primary concern. Due to the high-speed signals on the Rambus physical layer, great care must be used when designing even the simplest passive components. Cables, connectors, printed circuit board traces, and chip packages can degrade signal integrity. Once this happens, all sort of problems begin to occur. Crosstalk, reflections, glitches, logic errors, clock skew are just a few examples which can create havoc for the high-speed digital designer. The TDR technique highlights these unwanted signal reflections and allows improvement of signal integrity.

Time Domain Reflectometry waveform analysis can be used qualitatively or quantitatively. A quick measurement may be used without a calibration in order to locate a short or open. Since the oscilloscope is displaying the

length of time it takes the fast edge to propagate through the Rambus microstrip trace, is it useful to think of time as being equal to distance when doing TDR. The round-trip time from the step generator to the discontinuity automatically is divided by two by the scope, thus displaying the propagation delay one way. If the dielectric constant of the media is known, the exact distance to the discontinuity can be measured. Just as the timebase units on the

The shape of the reflected wave reveals the nature and magnitude of the mismatch

The loads shown at the right:

- a) OPEN
- b) SHORT

Where

Z_L = Load Impedance
 Z_0 = Characteristic Impedance of Transmission Line

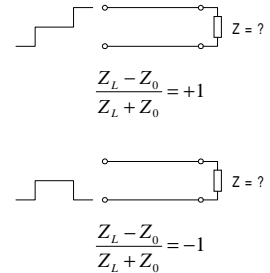
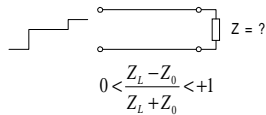


Fig.1 - Basic TDR Loads

oscilloscope may be changed from picoseconds to millimeters, the vertical units may be changed from millivolts to percent reflection. Since the amplitude of the original TDR step is known, any reflections can be expressed as a percent of the original. If impedance of the DUT is required, the vertical units may also be changed to ohms. The oscilloscope uses an impedance extraction algorithm embedded in firmware to accomplish these alternate units.

Let us now analyze the most basic circuit conditions, an open and a short. When the fast edge is launched into an open circuit, the reflected wave is equal in amplitude and the same polarity to the original. This produces a “double step” on the TDR waveform. The first part of the step on the display is the launched edge itself and the second edge is the reflection of the open. If a short is encountered in the DUT, the reflection is equal in amplitude and opposite in polarity. This produces a falling edge after the original launched edge. Recognizing these two simple reflections is the first stage to using TDR waveform analysis. As more complex loads are measured with TDR, the signal integrity engineer develops an intuitive database.

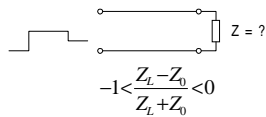
The shape of the reflected wave reveals the nature and magnitude of the mismatch



The loads shown at the right:

- a) $Z_L > Z_0$
- b) $Z_L < Z_0$

Where $\frac{Z_L - Z_0}{Z_L + Z_0}$



is Reflection Coefficient

Fig. 2 - Purely resistive TDR loads

Let us now consider a purely resistive load on a microstrip line with a characteristic impedance, Z_0 , of 50 ohms. If a narrower segment of microstrip is encountered, the impedance will increase from 50 ohms (this assumes no variation in the ground plane or dielectric constant in the local area). The corresponding TDR waveform for this higher impedance segment will be a double step with the size of the second step corresponding to the increase in impedance at the transition (50 ohms produces no reflection, an open results in 100% reflection). Likewise, if a wider segment of microstrip is introduced, the impedance will drop from 50 ohms and the TDR waveform will show a staggered step with the second level between that produced by a 50 ohm level (no reflection) and a short (minus 100%).

If we now consider an impedance discontinuity with real and complex components, we introduce something closer to an actual device³. A particular structure, such as a circuit board via, can add excess inductance or excess capacitance to the characteristic impedance of the microstrip line. If it is capacitive, it will appear to the fast edge at time $t = t_0^+$ as a short. This will create a TDR waveform that deflects in the negative direction from the characteristic impedance. After a number of time constants have passed, the waveform will return to a level value. This negative pulse is another key TDR waveform indicator for the experienced TDR user. In a similar fashion, if an inductive discontinuity is encountered, it will appear as an open circuit at time $t = t_0^+$. This will create a positive pulse, up from the 50-ohm level.

Rambus Characteristic Impedance

The Rambus microstrip can be easily spotted on the computer motherboard because of the wider trace width. This wider geometry was chosen to more closely match the impedance of the complete Rambus RIMM module when fully loaded with SDRAM silicon devices. By creating this controlled impedance environment, the Rambus architecture can exhibit lower reflections from impedance discontinuities. This enables the Rambus physical layer to achieve better signal integrity and therefore higher speeds.

Unfortunately, this geometry does not aid the circuit board manufacturers. In their ongoing quest to do things better, faster, cheaper and smaller, Rambus has created a technical challenge. The ability to control the impedance environment of Rambus is proving to be extremely challenging with existing circuit board fabrication technology. This has led to 100% board test for some vendors.

As mentioned previously, the TDR oscilloscope measures impedance versus distance with a familiar time domain interface. Highly accurate impedance measurements require a TDR calibration that sets the reference plane at the DUT's input. To address the most demanding impedance profile measurements, one should utilize a Digitizing Oscilloscope that allows the user to set this reference plane at the probe tips. By using the TDR Probe Kit shown in figure 3 below, a special calibration adapter enables a precision 50-ohm air dielectric termination and SMA short to be attached to the probe tip.



Fig. 3 – TDR Probe

Probing with Enhanced Accuracy

When attaching any test instrumentation to a Device Under Test (DUT), the test fixturing utilized always affects the measurement in some fashion. TDR test fixturing is no exception. Whether probing or launching from an SMA connector, there are anomalies and impedance discontinuities located within the test fixture which inherently contribute to measurement error. With a TDR measurement, this is directly translated into error in impedance.

The Direct Rambus™ microstrip trace needs to be maintained to 28 ohms +/- 2.8 ohms. Enhancement of standard TDR waveforms is needed to ensure compliance to this standard along the complete length of the Rambus channel. As seen in the figure below, the standard TDR waveform depicts reflections from the DUT using the internal 40-picosecond TDR step generator.

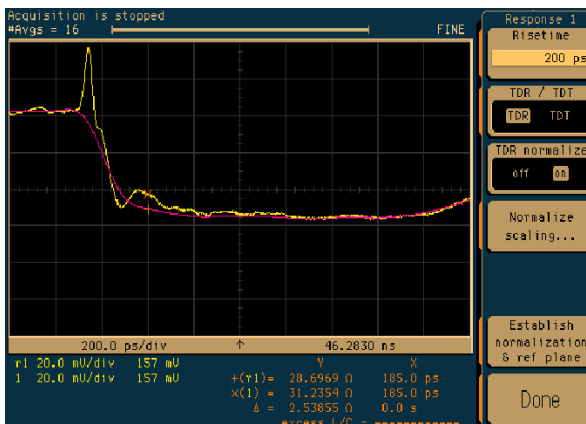


Fig. 4 – Rambus RIMM Impedance Profile

superimposed waveform is the normalized waveform that corrects for test fixture anomalies. The very beginning of the 28-ohm microstrip section has artifacts at the "knee" which are not characteristic of the DUT. When viewing the normalized waveform, these artifacts have been corrected, thus yielding an enhanced accuracy impedance measurement.

Normalization Process

The method of TDR calibration used for setting the reference plane at the probe tip is a two-point calibration using a precision 50-ohm and a short. Utilizing the powerful processing

power of modern Digitizing Oscilloscopes, the instrument performs a Fast Fourier Transform to transform the time domain waveform into the frequency domain⁴. The calibration data is then used to create a digital filter for correcting the errors introduced by the test cable, probe and probe tip. An Inverse Fast Fourier Transform is then performed to bring the frequency spectrum back into the time domain and this is what is displayed as the normalized waveform. This

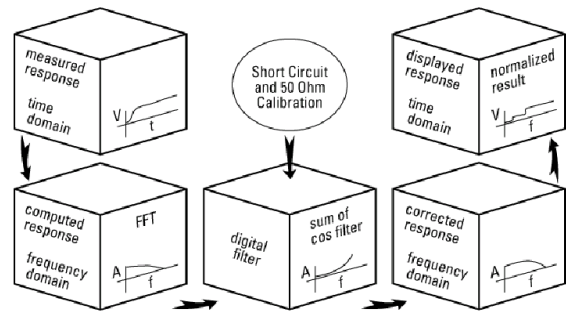


Fig. 5 – Normalization Process

deconvolution of the frequency domain information is displayed in real time to give the look and feel of a standard scope channel. A graphical representation of this process is shown in figure 5.

TDR Modeling Software

As a complement to the normalization built into the Digitizing Oscilloscope, the authors used another helpful signal integrity tool, IConnect™ software by TDA Systems. While normalization corrects for error due to test fixturing, the TDR software corrects for multiple reflections within the DUT itself.

For Rambus applications, these reflections may not be very pronounced (such as measurement of the impedance on the continuity board). However, the reflections may play important role in measurements of populated Rambus memory module. In order to remove the effects of multiple reflections, the TDA Systems IConnect™ software implements an impedance deconvolution algorithm. This algorithm is applied to the normalized TDR waveform.

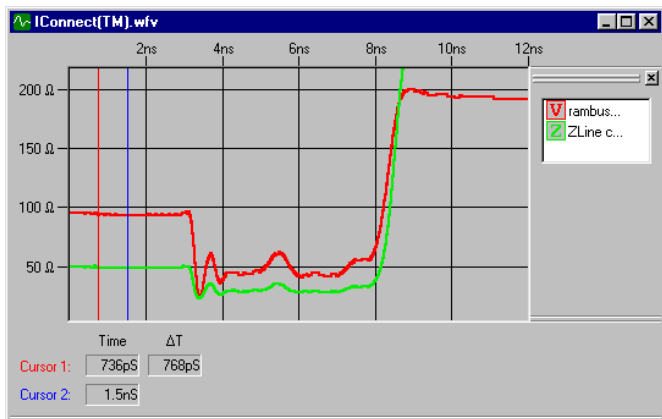


Fig. 6. - IConnect™ Impedance profile

The TDR waveform can be directly imported into the IConnect™ software via the GPIB interface in the Hewlett Packard 54750A TDR oscilloscope. The resulting true impedance profile waveform takes into account multiple reflection effects. Furthermore, by extracting and verifying the SPICE model using IConnect™ software, a board designer can ensure the highest level of confidence in the accuracy of the impedance values obtained using TDR measurements.

SPICE Models from TDR

From the true impedance profile, direct readouts of line impedance, time delay, capacitance and inductance can be obtained. Based on the true impedance profile waveform, IConnect™ software can automatically compute the SPICE model for the DUT and save this model to a file in order to be reused in further system simulations. A sample printout of such file is given in the Appendix I. Finally, the model can be verified through simulation using an integrated interface to SPICE in the IConnect™ software. Models for TDR measurement source and termination are generated in the software in order to match the measurement stimulus and termination conditions.

High level of correlation between simulation and measurement results in high confidence for the designer in the accuracy of the model.

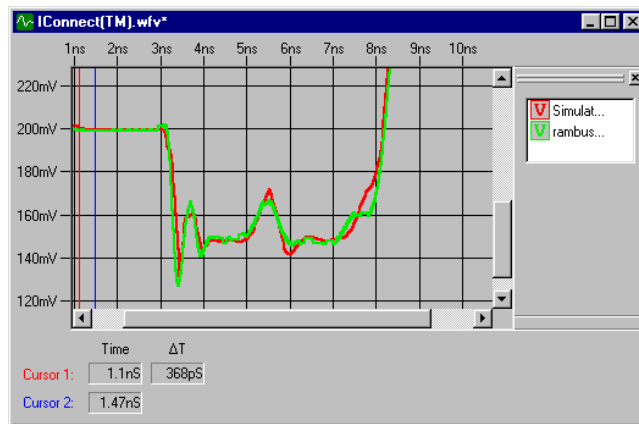


Fig.7 - Measured and simulated waveforms in the IConnect™ software.

The measured and simulated waveforms can be directly compared in the same waveform viewer, resulting in easy model verification. If the initially computed model values do not result in perfect match between simulation and measurement, the board designer can then refine the computed SPICE model, re-simulate it and achieve the desired level of fit of the model to the measurements. All this is done without leaving the framework of the IConnect™ software, resulting in rapid SPICE model extraction that accurately represent the behavior of the DUT in the system simulations.

IConnect™ software also allows modeling of coupling in the adjacent lines on the board. Once self and mutual capacitance and inductance values have been computed using IConnect™ software, a lumped coupled model can be generated that will accurately predict coupling behavior of the lines.

Rambus Measurements

Various configurations of the Rambus architecture were measured with a Digitizing Oscilloscope. TDR measurements were made on the motherboard and on stand-alone CRIMM's (Continuity Rambus Inline Memory Modules). Also, eye diagram measurements were made on the Rambus data lines. Both Read and Write operations were analyzed with eye diagrams with interesting results. First, the TDR waveforms are presented.

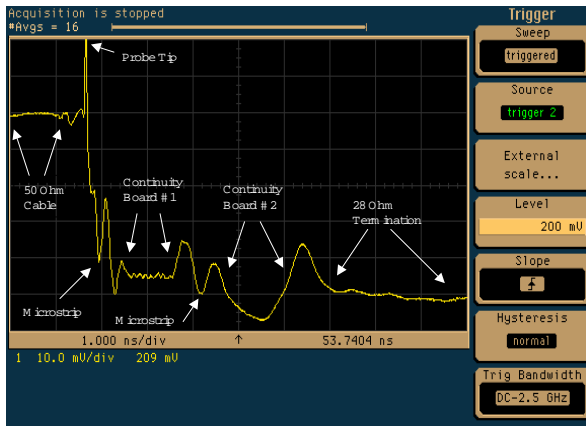


Fig.8 – TDR of Rambus Motherboard

The TDR waveform in Fig. 6 above was measured on a computer motherboard running Rambus. It shows the physical layout as seen by the 40ps risetime pulse generator in the HP TDR module. The TDR step is launched from the memory controller side of the Rambus RIMM's. As one can see, the waveform starts with the 50 ohm coax cable connected the TDR Probe. The waveform indicates an inductive impedance discontinuity at the probe, then it drops down to a short segment of motherboard into the Rambus connector. Plugged into this connector is the CRIMM. It is similar to a DIMM (dual in line memory module) and exhibits the same characteristic impedance as the Rambus itself (28 ohms).

Notice the section of the TDR waveform after the probe tip discontinuity. The TDR trace falls rapidly to the 28-ohm characteristic impedance of the first RIMM, but on either side of the 28-ohm "shelf" there seems to be some ringing. This is actually the impedance mismatch of the RIMM connector on the motherboard. Looking more closely, the positive going bump is most likely the excess inductance of the connector pins, while the negative going bump is the excess capacitance of the solder pad to which the pin is connected. The impedance variation through this connector interface is significant.

Moving along the TDR waveform further, a large valley can be noticed. This section of the TDR waveform shows lower impedance than 28-ohms and indicates a RIMM module out of specification and then finally the 28 ohm termination. If this motherboard were perfect, the characteristic

impedance would be a flat 28-ohms across the screen (after the probe tip 50-ohms). This motherboard needs some improvement for reliable operation at the full 1.6Gbytes per second speed.

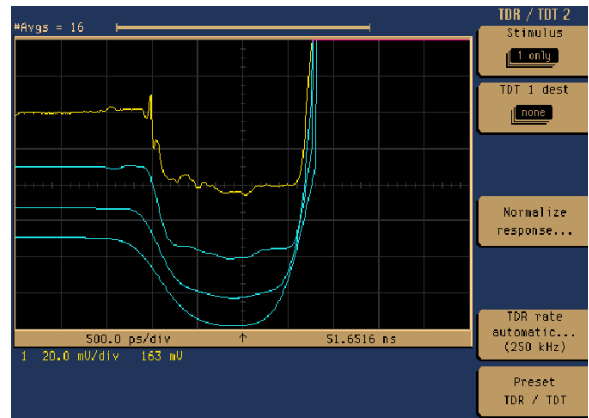


Fig. 9 – Stand alone CRIMM

When making signal integrity measurements of Rambus with a TDR oscilloscope, it is sometimes useful to look at the effective impedance profile at various risetimes. The top TDR waveform in Fig. 7 above represents the impedance profile of a CRIMM with the standard 40 picosecond risetime step generated from within the TDR plug-in module. This view shows the most detail and the largest reflections.

It is sometimes useful to see how the signal integrity improves with slower risetimes. If the data rate that the CRIMM would see in the real world has less high frequency content than represented by a 40 picosecond risetime step (it does), then we can simulate this with our TDR.

By setting the reference plane at the TDR probe tip as discussed earlier, one can deconvolve out the test fixture (cable + probe) and the simulate various risetime responses. This enhances TDR measurement accuracy by minimizing the initial impedance discontinuity of the probe tip (typically excess inductance due to ground lead). The risetimes simulated here are 200, 400 and 600 picoseconds (200 picoseconds being the de facto Rambus standard). Note these slower risetimes exhibit what we would expect: lower reflections from slower edges.

The TDR waveform in figure 10 shows a shape comfortably typical of a CRIMM.

However, upon further investigation of the impedance profile, the CRIMM looks like it is only 14 ohms. What is happening? Thinking about the bus structure, we have chosen a TDR launch point that is in the middle of the bus. The

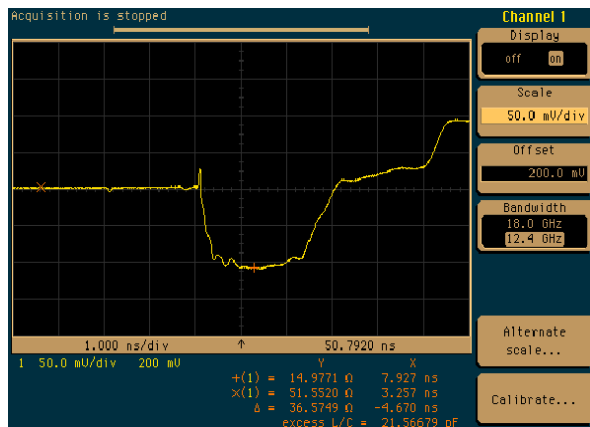


Fig. 10 – Two 28 ohm stubs in parallel

last CRIMM is disengaged, so it is known that the terminating resistors are disengaged from the circuit. The memory controller chip is located at the other end of the bus. This chip is turned off, so it has an effective impedance that is quite high. So high, it is practically an open circuit. So, if one is probing in the middle of a 28-ohm section of microstrip that is open on both ends, this is effectively two 28-ohm resistors in parallel. This is why the TDR measures 14 ohms, not 28-ohms as expected.

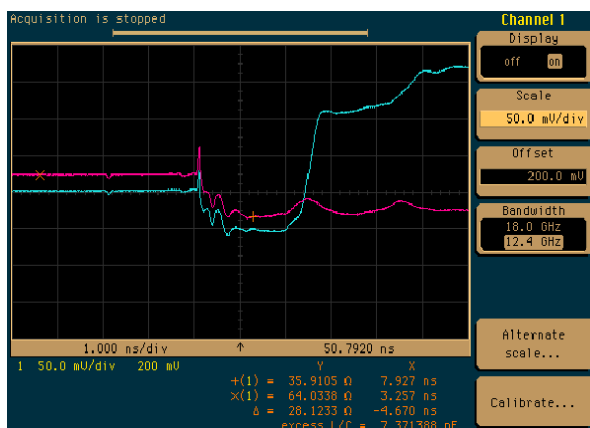


Fig 11 – Charging up V_{ref} plane

The TDR waveform shown in figure 11 above indicates the effect of launching a TDR

step into Rambus when the 28-ohm terminating resistor is engaged. This condition exists when probing from the memory controller side of the bus and all RIMM modules are plugged into the motherboard.

The blue (bottom) waveform is stored in memory and represents a measurement taken with the last RIMM removed. This creates an open circuit between the memory controller chip and the terminating resistors, thus giving an accurate assessment of the CRIMM impedance profile. Things to notice are the 50-ohm coax, the inductive discontinuity of the probe tip, the 28 ohm characteristic impedance of the CRIMM trace and then lastly the open circuit. However, if we now plug the last CRIMM into place and launch our TDR step into the same exact location as before, we get something very curious.

Looking at the red waveform, we see that whole waveform is shifted up slightly. The termination resistors are visibly engaged, so that makes sense. But looking at the markers located at the CRIMM location, it tells us the new impedance is 36 ohms. Furthermore, the coax marker tells us that the coax cable is now 64 ohms. Did we lose calibration somewhere? The answer is no. What is happening is this: the terminating resistors are not terminated into ground in the Rambus topology. Unlike the typical terminations into ground that we are used to seeing, the Rambus microstrip is terminated into a voltage plane on the motherboard. This voltage plane effectively becomes one side of a parallel plate capacitor with the ground plane and dielectric material in between. The repetitive TDR step is actually charging up the capacitor. This pulls up the voltage and creates a DC offset that the TDR interprets as a larger reflection and therefore higher impedance.

Conclusion

High-speed digital designers can no longer ignore transmission line effects of PCB microstrip traces. New high bandwidth bus architectures, such as Direct Rambus™, will continue to challenge designers. To understand and solve signal integrity issues, a high bandwidth oscilloscope with TDR capability is an

intuitive measurement tool capable of handling the job.

Acknowledgments

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References:

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Appendix I

Sample printout of a SPICE model file generated using IConnect™ software

```
* Time Domain Analysis Systems: IConnect™
* File Created: March 16, 1999 at 01:50PM
* Created By: Dima Smolyansky
* Format: Model
* Type: Single Line
* Z Waveform: ZLine calibrated.wfm
* Partition: 862p, T-Line, Right Edge, 1, 0, 0
* Partition: 3.11n, T-Line, Mean, 1, 49, 1.13n
* Partition: 3.88n, CL, Right Edge, 1, 4n, 3p
* Partition: 5.32n, T-Line, Mean, 1, 28.5, 900p
* Partition: 5.67n, L, Right Edge, 1, 3n, 5.41p
* Partition: 7.54n, T-Line, Min, 1, 28, 933p
* Partition: 8.01n, T-Line, Left Edge, 1, 32.5,
239p
* Syntax: PSpice
* Name: Automatically Generated
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t1 port1 gnd_ 2 gnd_ Z0=49 TD=1.13n
c2_0 2 gnd_ 3p
l2_1 2 3 4n
t3 3 gnd_ 4 gnd_ Z0=28.5 TD=900p
l4 4 5 3n
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t6 6 gnd_ port2 gnd_ Z0=32.5 TD=239p
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